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NEC:ROPROS

NEC:Poseidon

MS-7410 uATX

Version: 12

CPU: Intel, Socket 775 (Intel Core 2 Duo Processors, Intel Pentium D Processors, Intel Pentium 4 Processors, Intel Celeron D Processors)-- 65-95 watts Intel Core 2 Duo, Pentium D, Celeron D

System Chipset:
Intel Bearlake - G (G33) (North Bridge)
Intel ICH9 Series (South Bridge)
ROPROS-MA use ICH9 / **ROPROS-VS use ICH9DH / Poseidon use ICH9R**

On Board Device:
CLOCK Gen -- SLG84516BT CLK Gen.
LPC Super I/O -- SCH5617
LAN -- Broadcom-BCM5787M (only MA) **LAN -- INTEL 82566 (Support ViiV)**
HD Audio Codec -- ALC262 VER:C2
TPM - SLB9635







Main Memory:
Dual-channel DDR-II * 4


Expansion Slots:
PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT * 1
PCI SLOT * 2

PWM: VRD11 Intersil 6312 3Phase

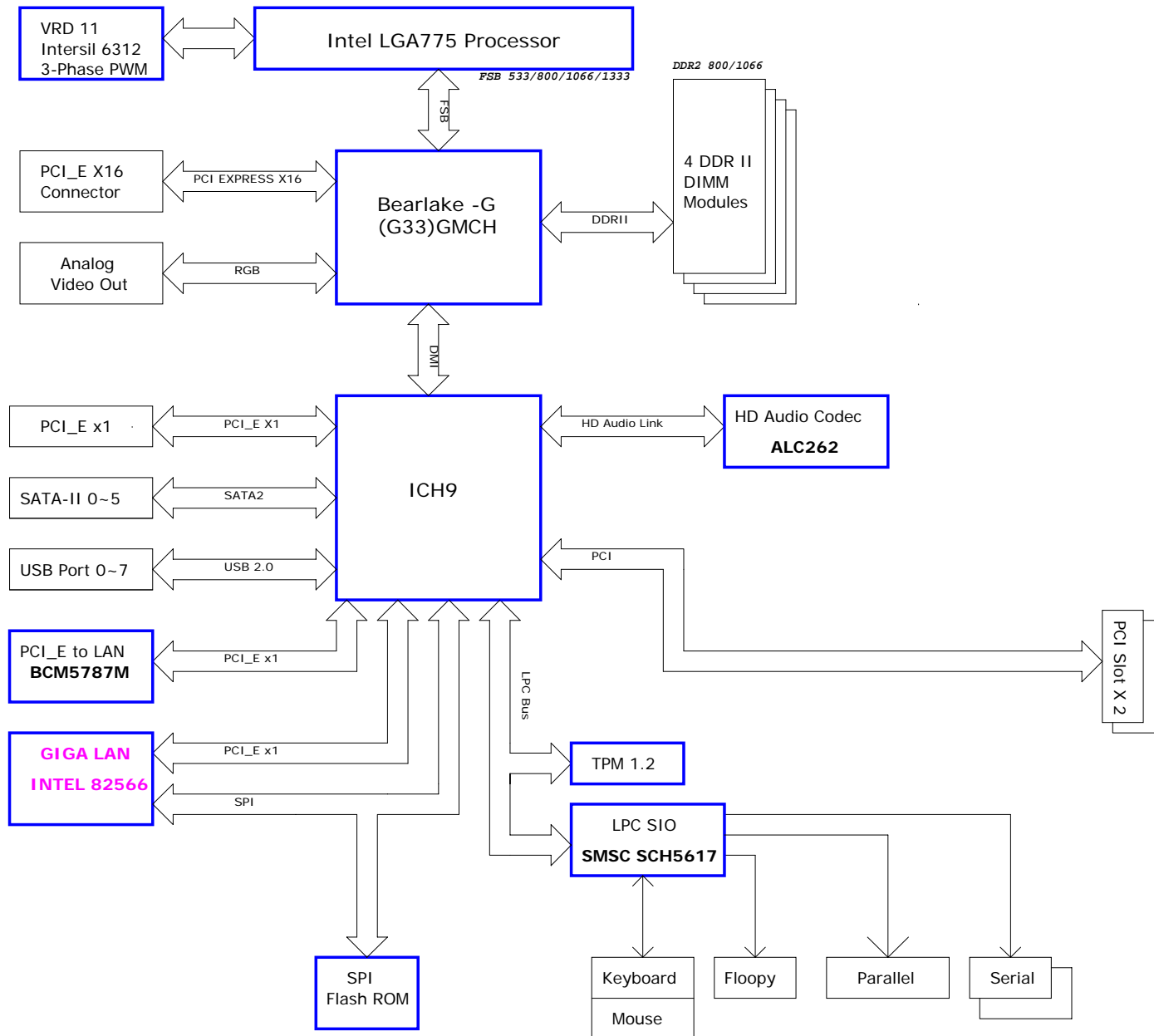


How to distinguish the different SKU

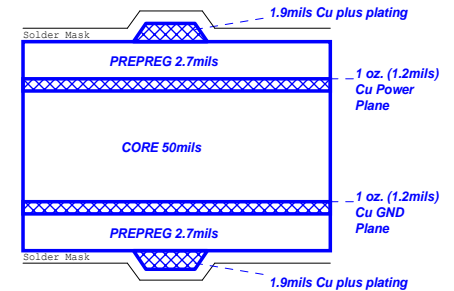
	BLUE Color which mean all model need use
	ORANGE Color which mean ROPROS-MA use
	PINK Color which mean ROPROS-VS
	DEEP GREEN Color which mean Poseidon
	PURPLE Color which mean ROPROS-VS & Poseidon
	BROWN Color which mean the part reserve

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Block Diagram



Board Stack-up (1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
 USB2.0 - 90ohm : 15/7.5/4.5/7.5/15
 SATA - 95ohm : 15/8/4/8/15
 LAN - 100ohm : 15/10/4/10/15
 PCIe - 95ohm : 15/8/4/8/15

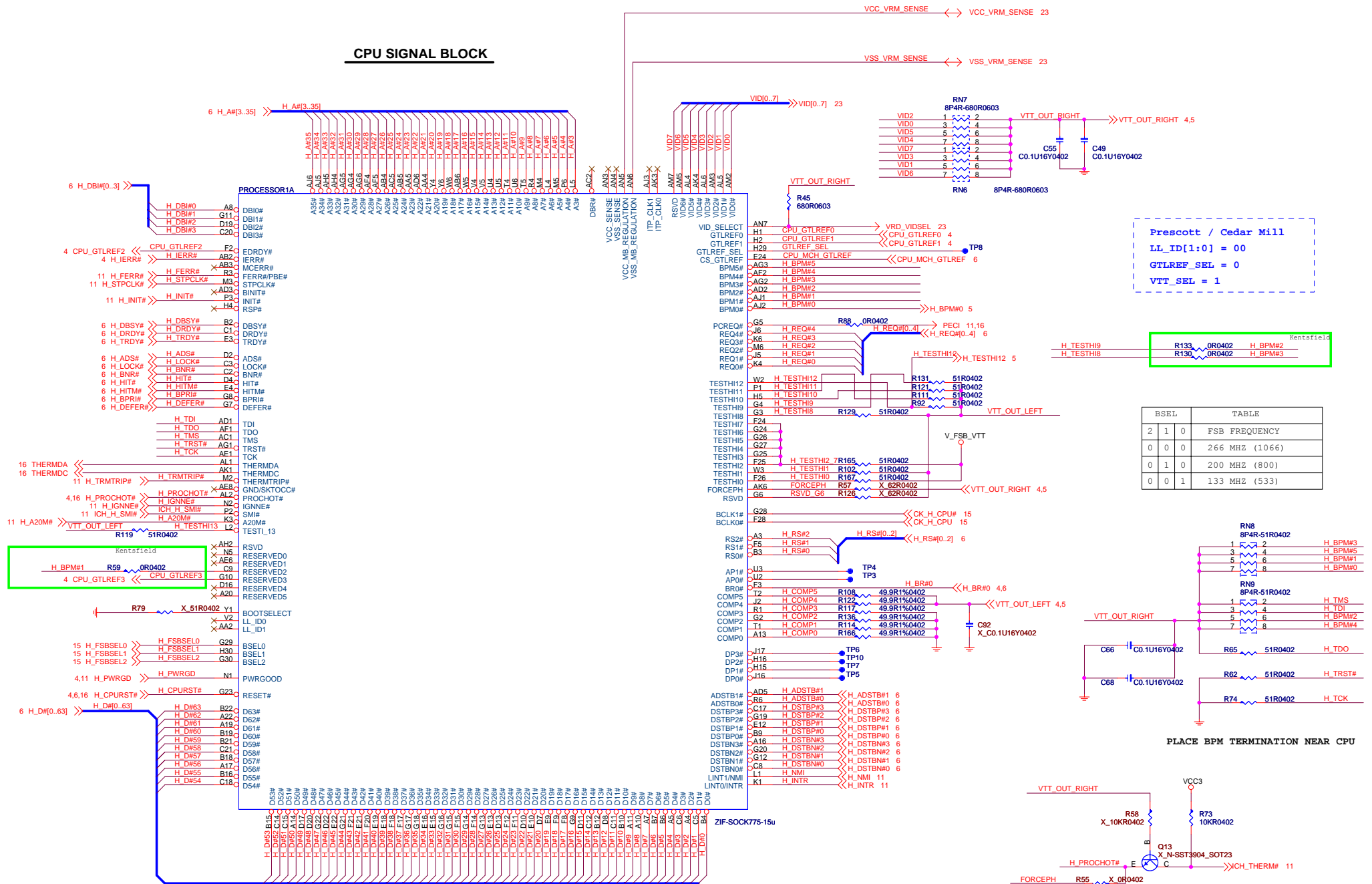


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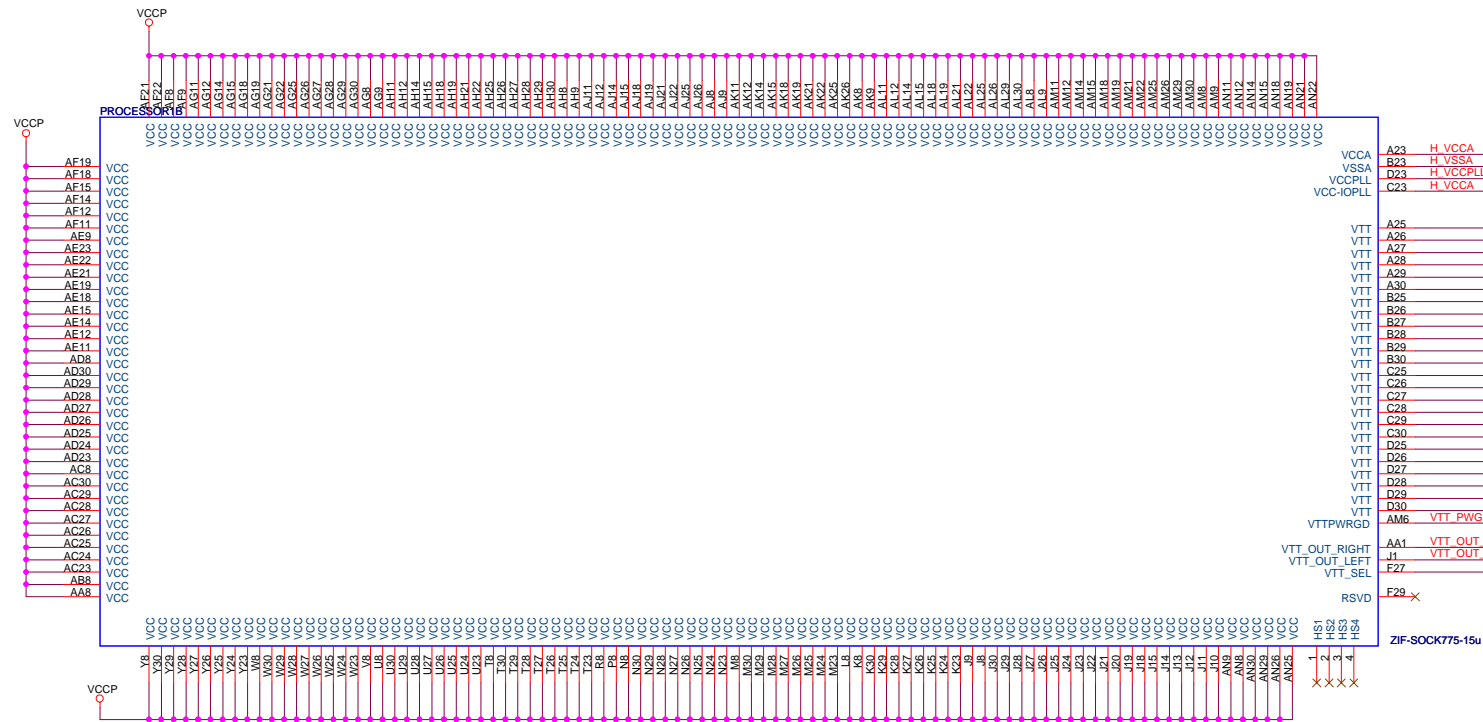
CPU SIGNAL BLOCK



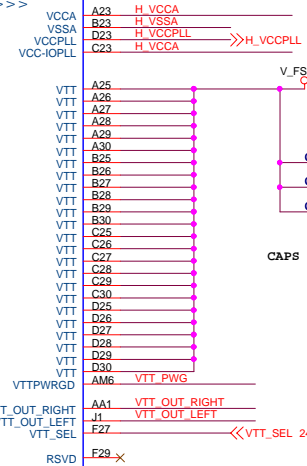
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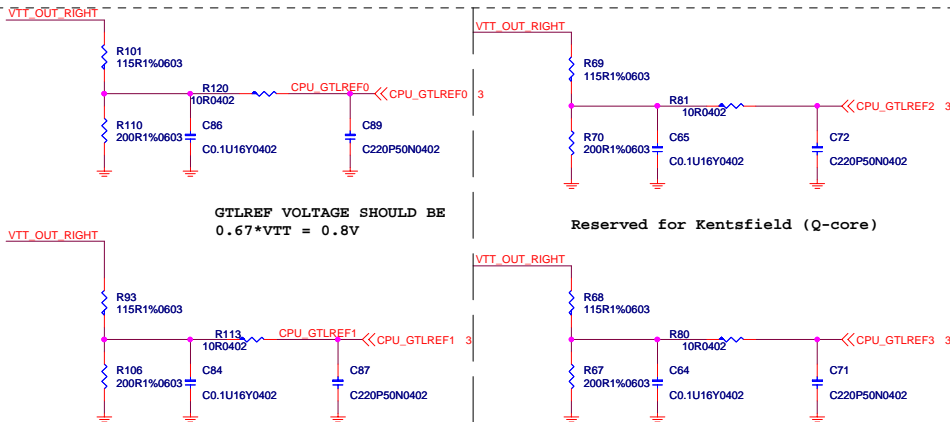
VCCA ----- 120mA
VCCIOPLL --- 100mA



CAPS FOR FSB GENERIC

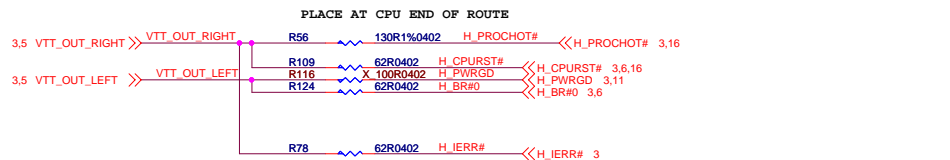
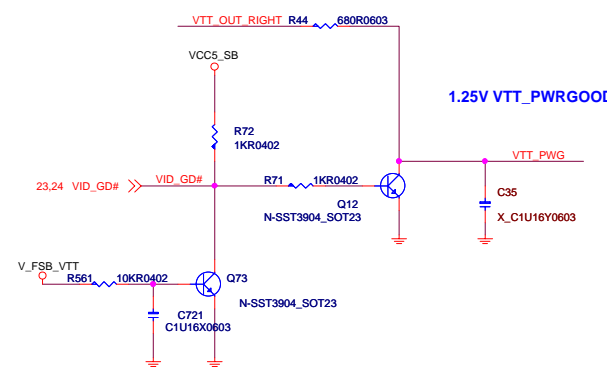
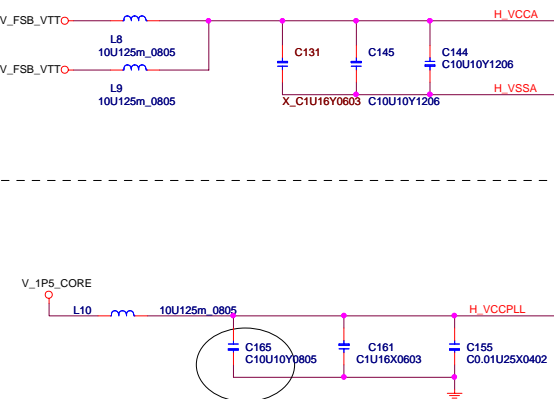


VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns



PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET

TRACE WIDTH TO CAPS MUST BE SMALLER THAN 12MILS

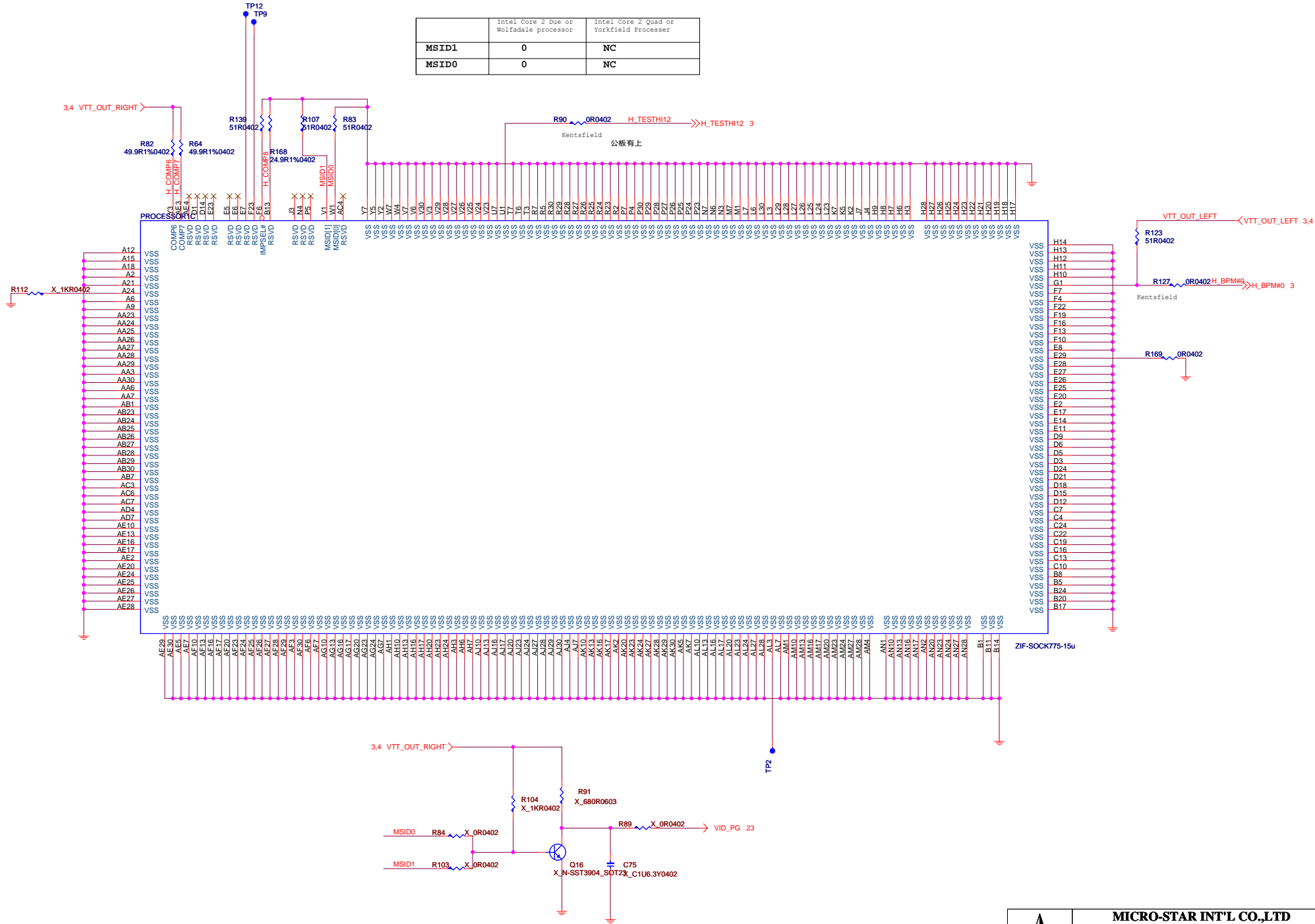


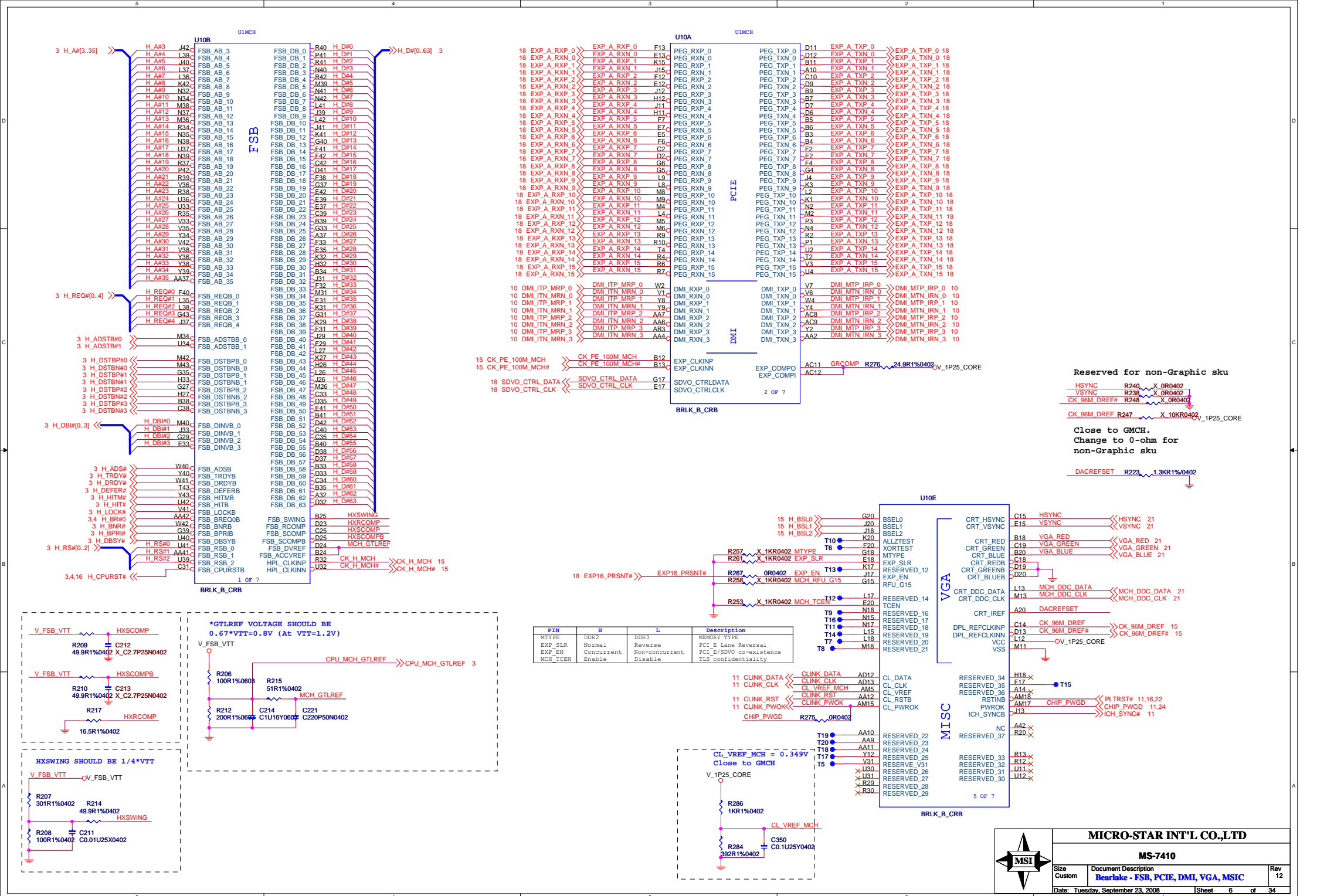
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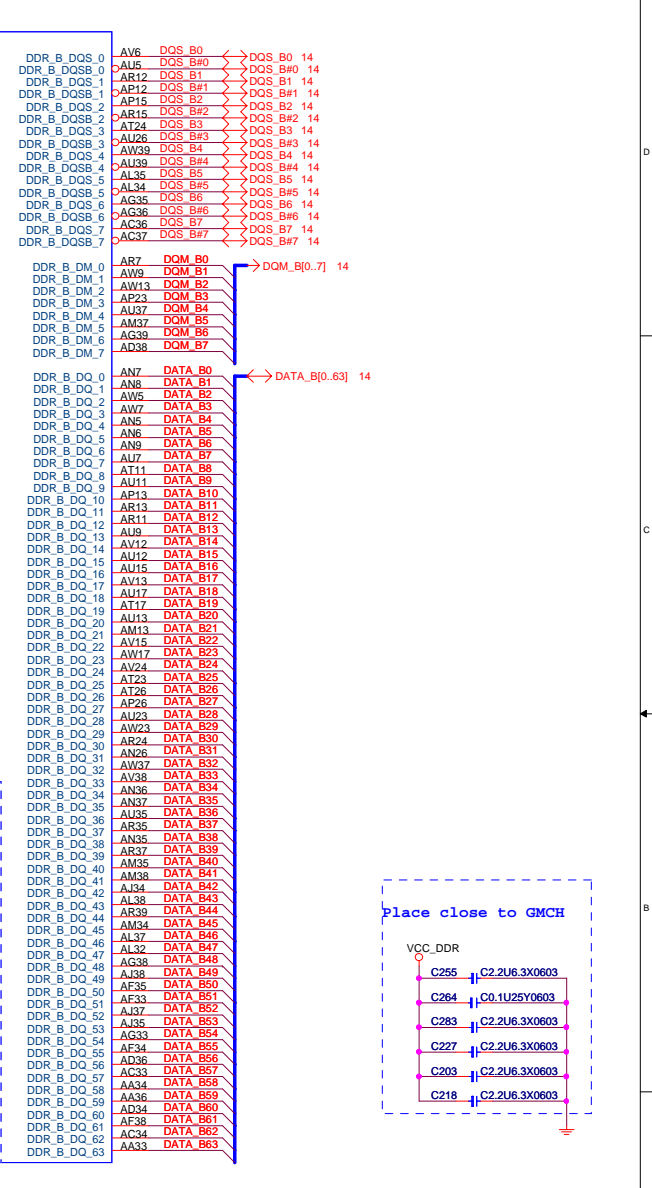
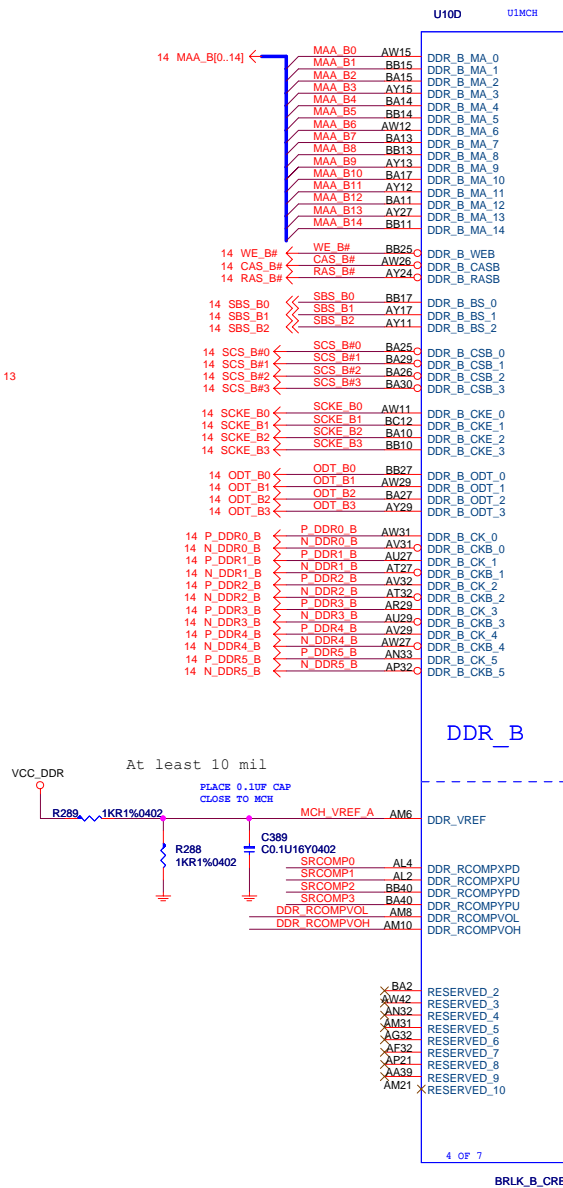
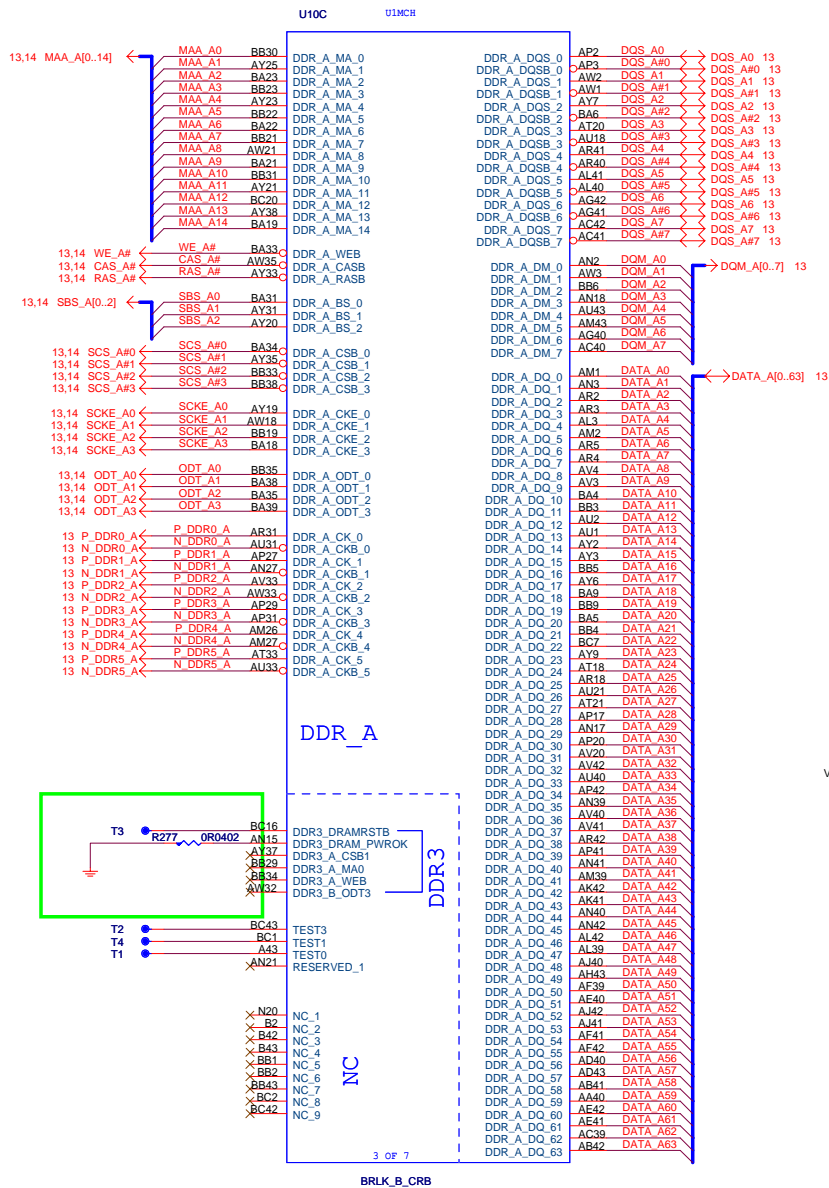
MS-7410

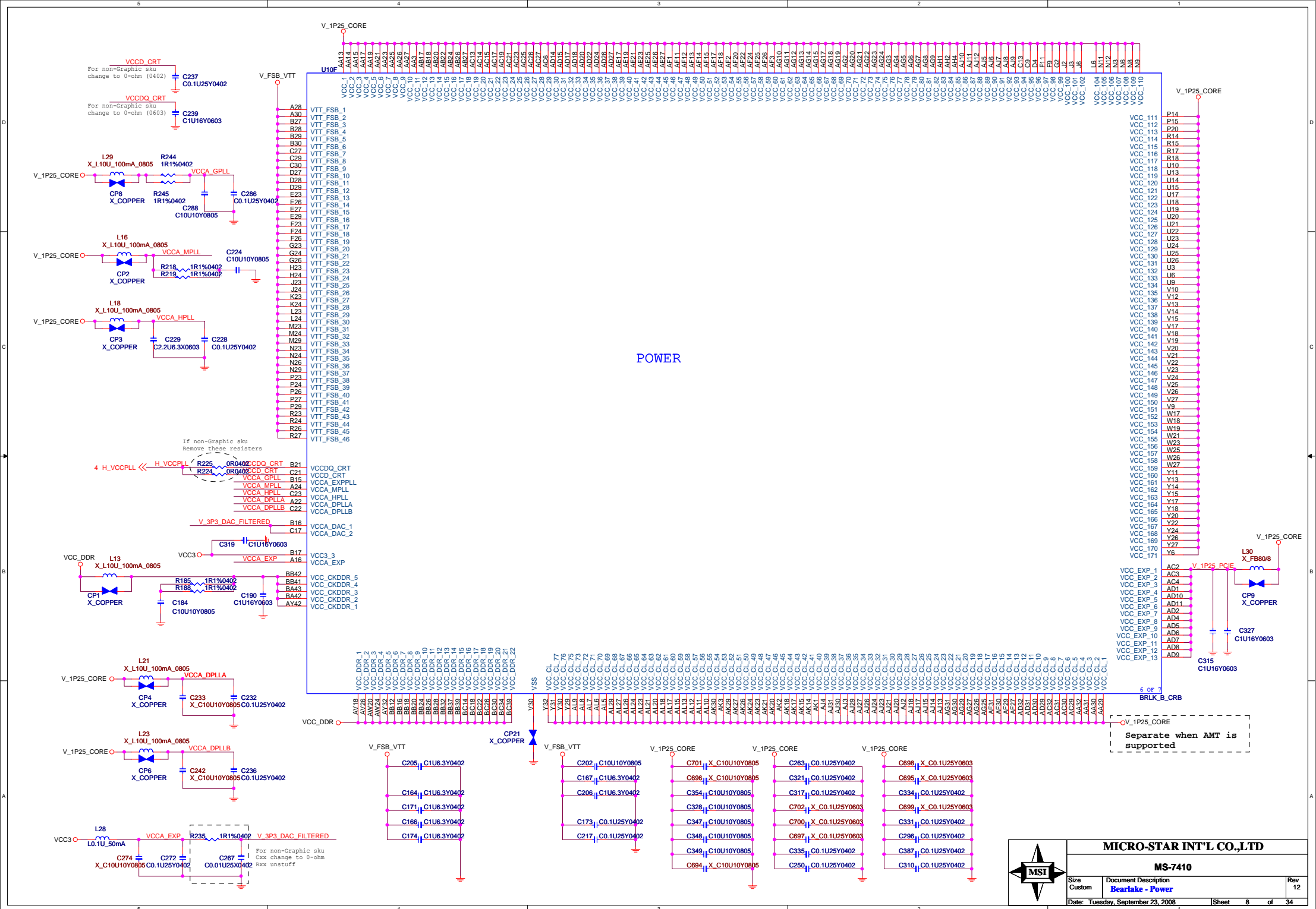
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Custom	Intel LGA775 CPU - Power	12
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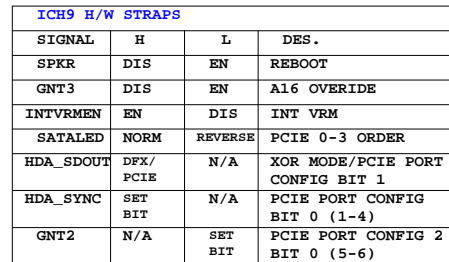
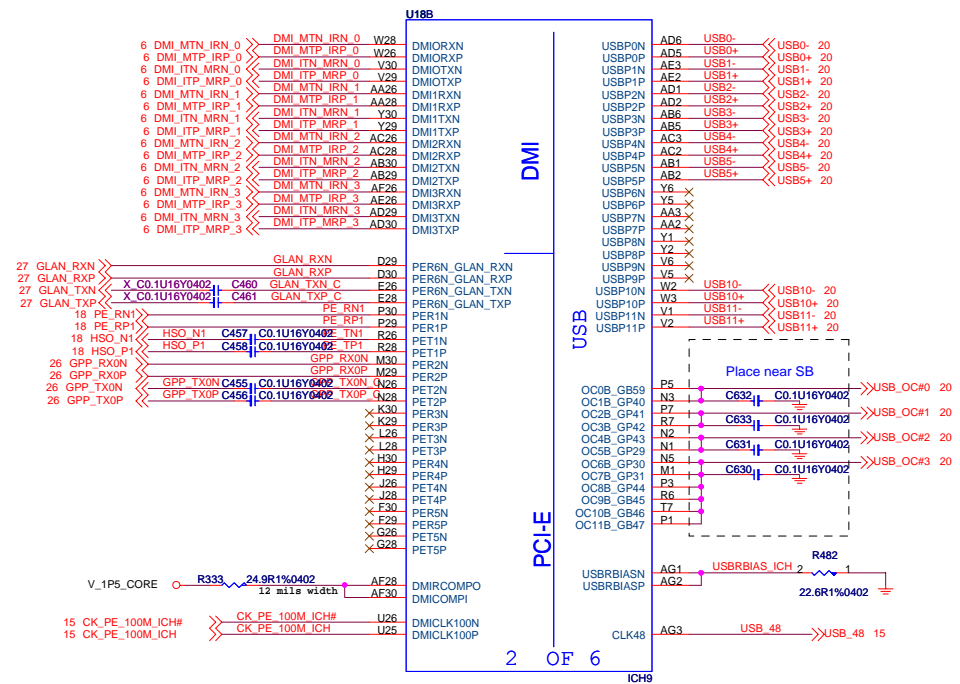
	Intel Core 2 Due or Wolfdale processor	Intel Core 2 Quad or Yorkfield Processor
MSID1	0	NC
MSID0	0	NC





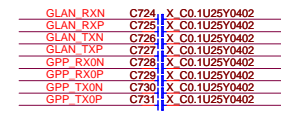


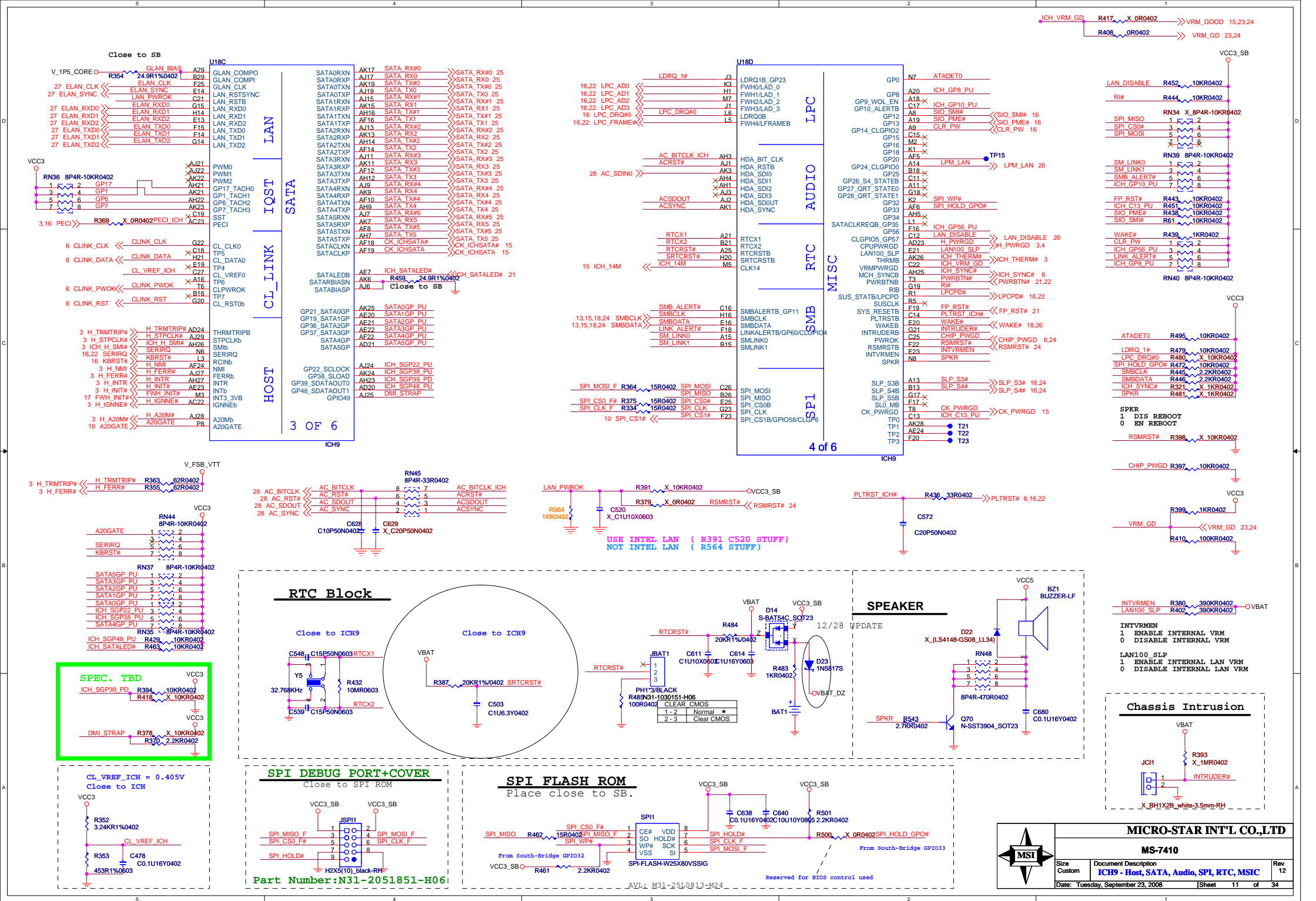




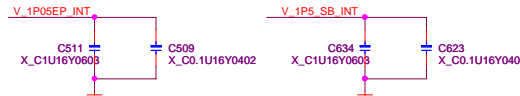
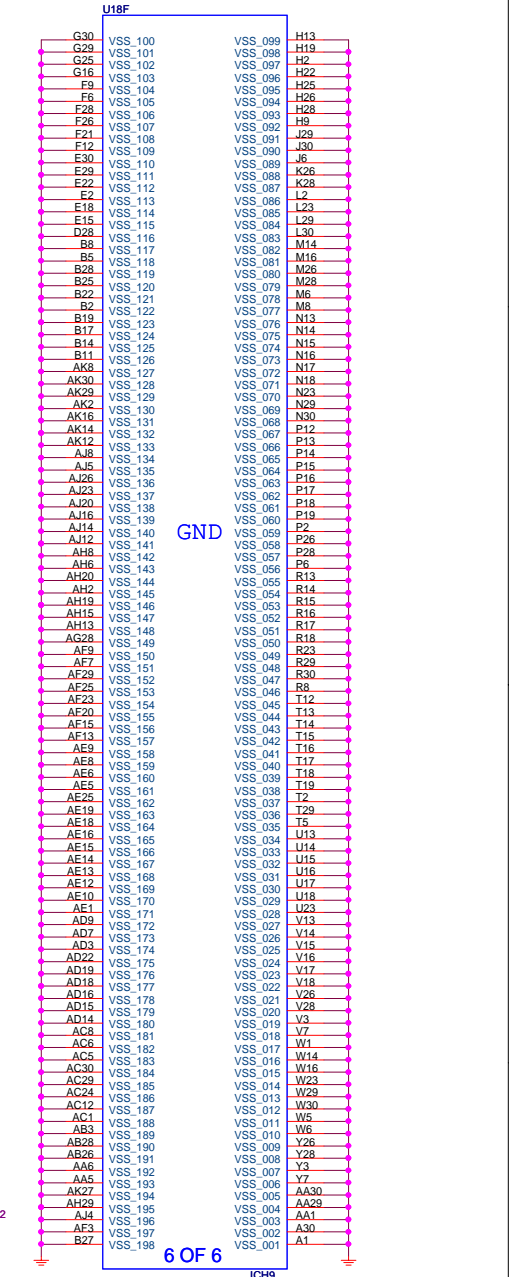
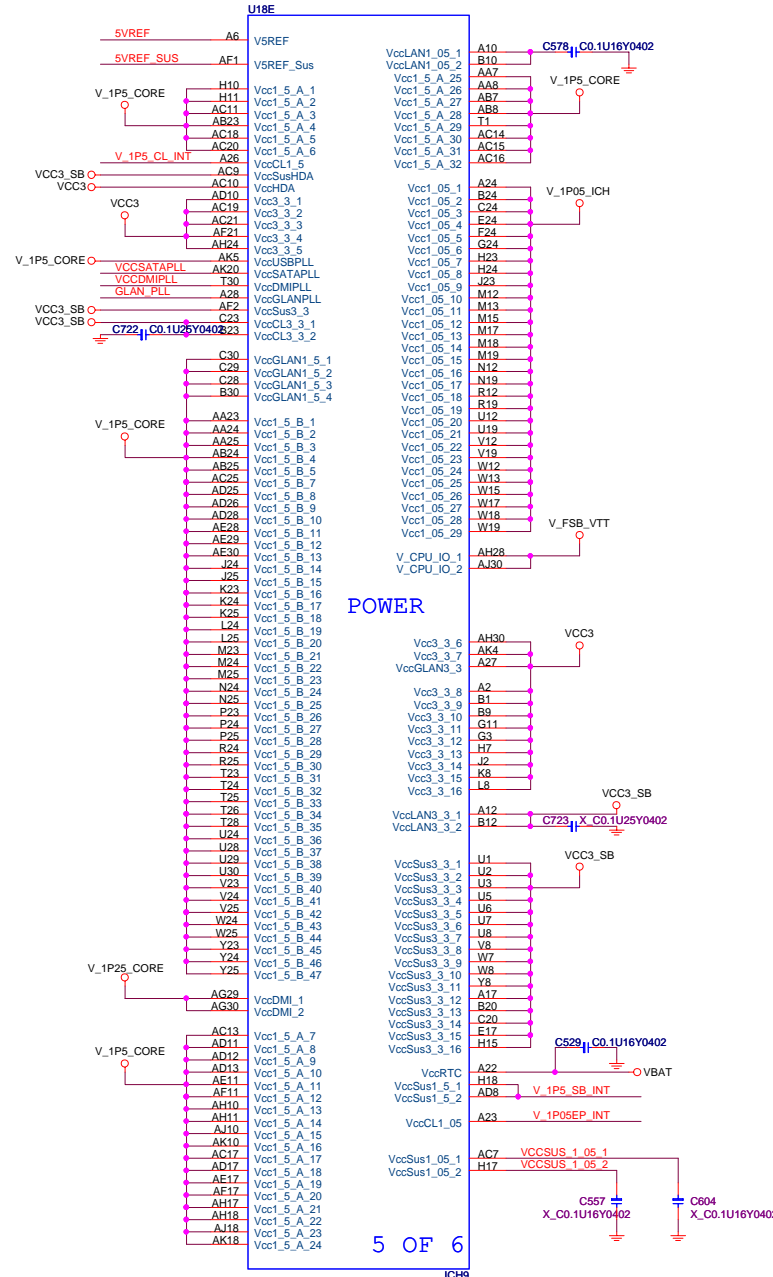
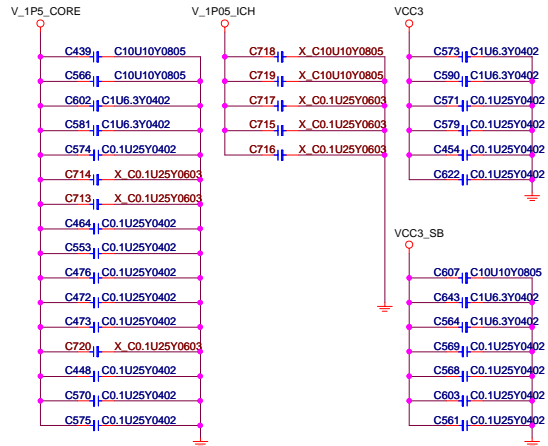
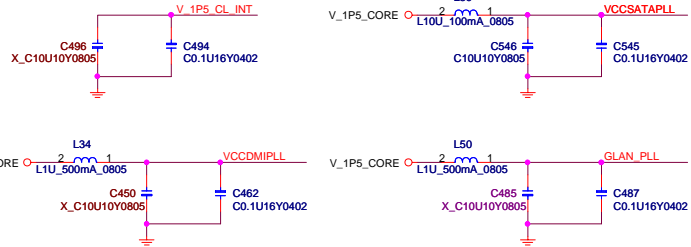
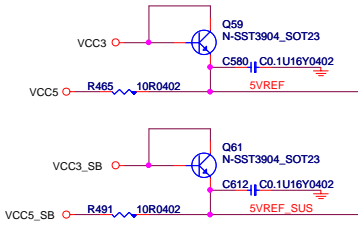
BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
FWH	1	1
SPI	0	X
PCI	1	0

SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERRIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)





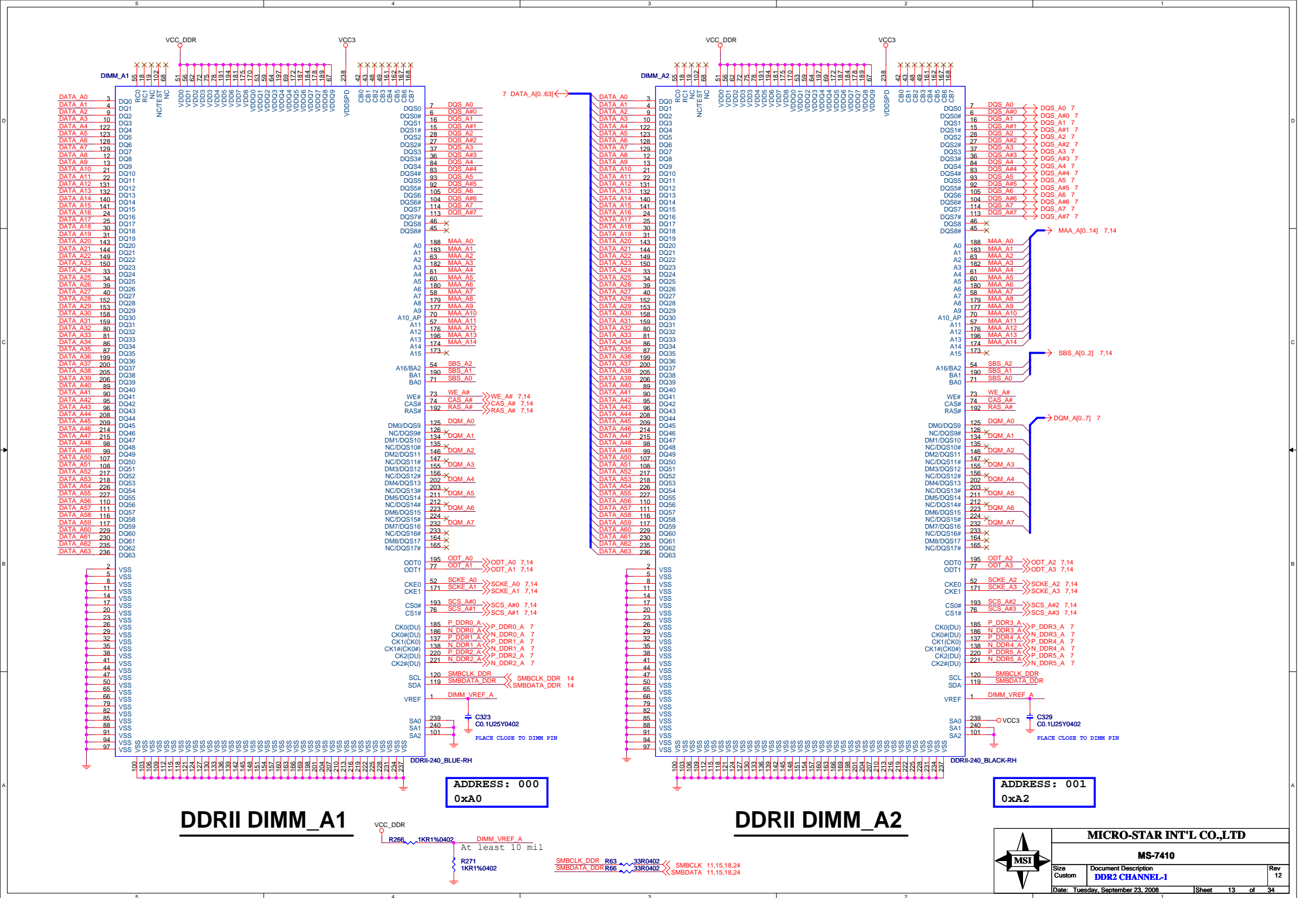
5VREF & 5VREF_SUS Sequencing Circuit

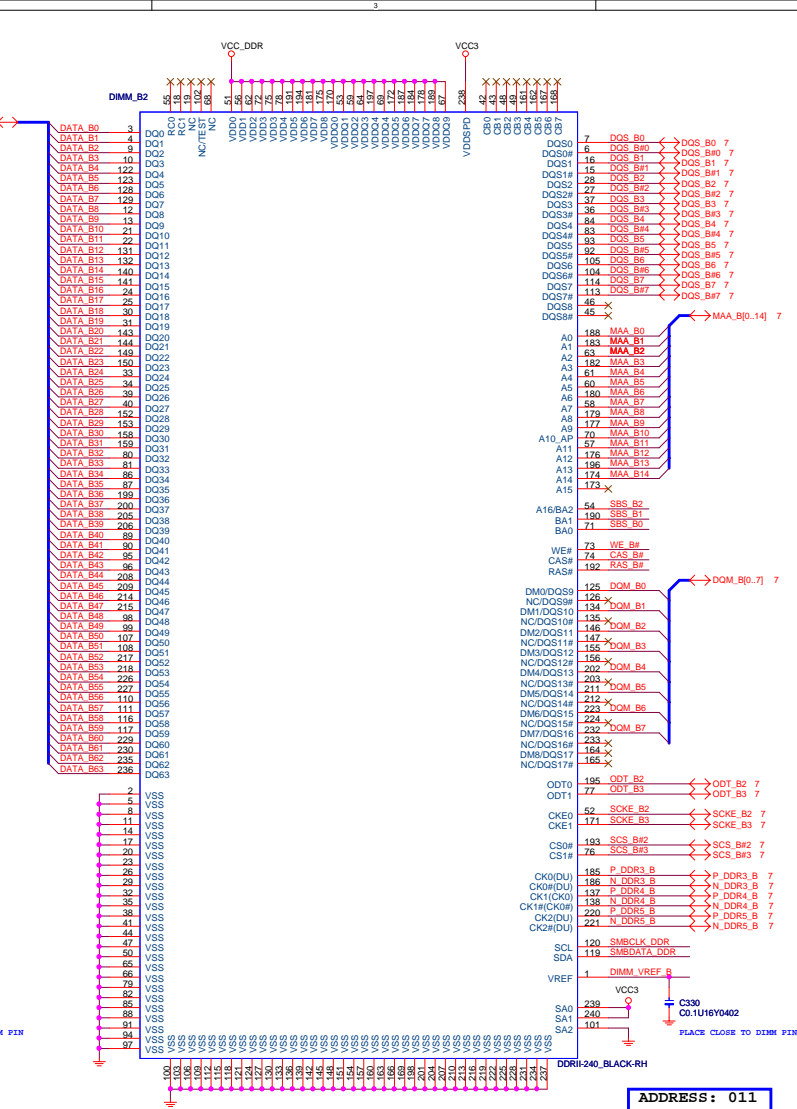


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VCC_DDR

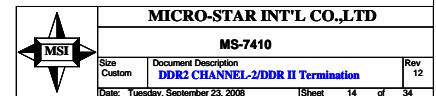
R265 1KR1%0402

DIMM VREF B

At least 10 milliohms

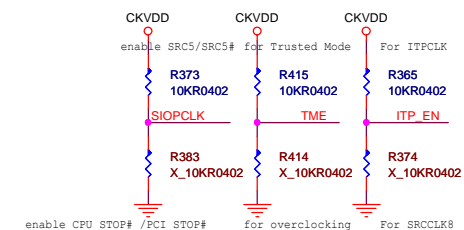
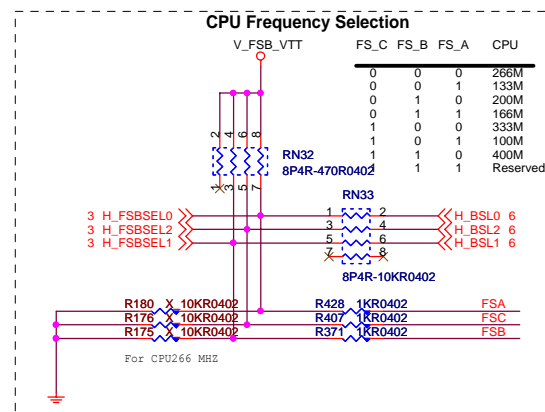
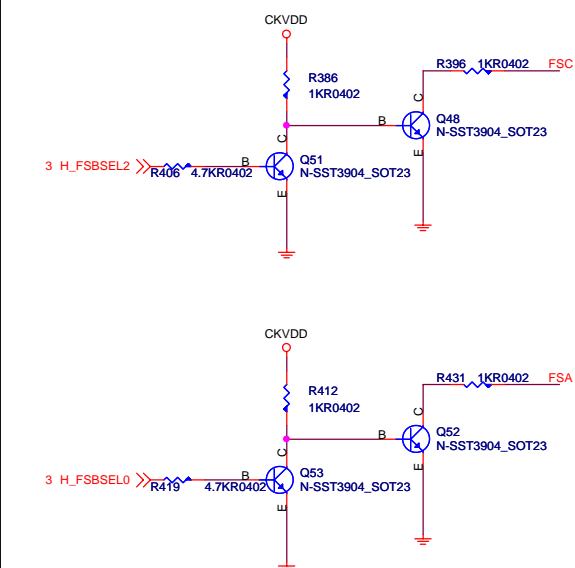
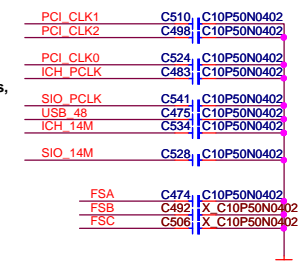
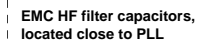
R270 1KR1%0402

ADDRESS: 011
0xA6



PCB layout showing HF filter capacitors placed close to the PLL. The diagram includes two main sections: one for the CKVDD_IO supply and another for the CKVDD supply. Each section shows a series of capacitors connected to a common ground plane. The capacitors are labeled with their values and part numbers. A table at the bottom lists the capacitors and their connections.

Component	Value	Part Number
CKVDD_IO	0.1uF	C428
CKVDD	0.1uF	C526
CKVDD	0.1uF	C468
CKVDD	0.1uF	C507
CKVDD	0.1uF	C437
CKVDD	0.1uF	C488
CKVDD	0.1uF	C525
CKVDD	0.1uF	C431
CKVDD	0.1uF	C425
CKVDD	0.1uF	C426
CKVDD	0.1uF	C430
CKVDD	0.1uF	C427
CKVDD	0.1uF	C422
CKVDD	0.1uF	C432
CKVDD	0.1uF	C483
PCI_CLK1	0.1uF	C510
PCI_CLK2	0.1uF	C498
PCI_CLK0	0.1uF	C524
ICH_PCLK	0.1uF	C483
SIO_PCLK	0.1uF	C541
USB_48	0.1uF	C475
ICH_14M	0.1uF	C534
SIO_14M	0.1uF	C528
FSA	0.1uF	C474
FSB	0.1uF	C492
FSC	0.1uF	C506

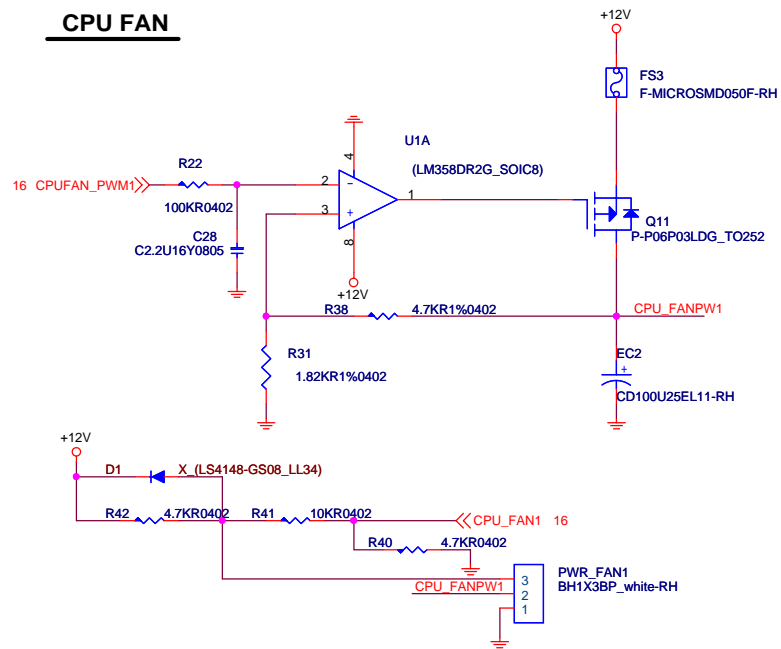


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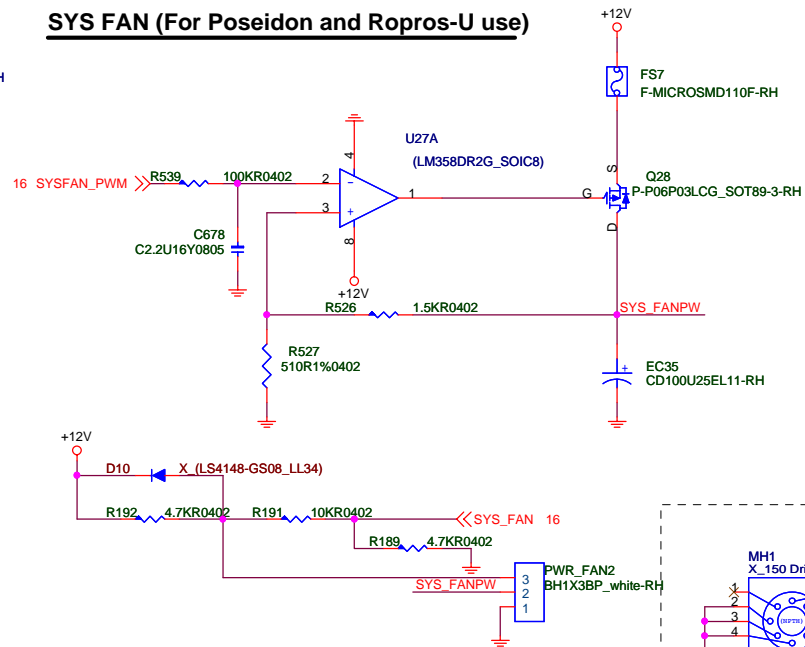
Rev	12
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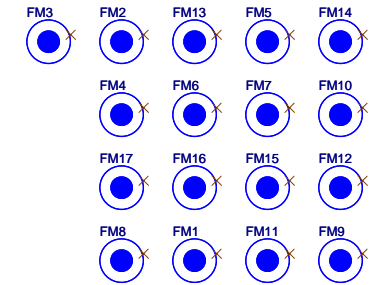
CPU FAN



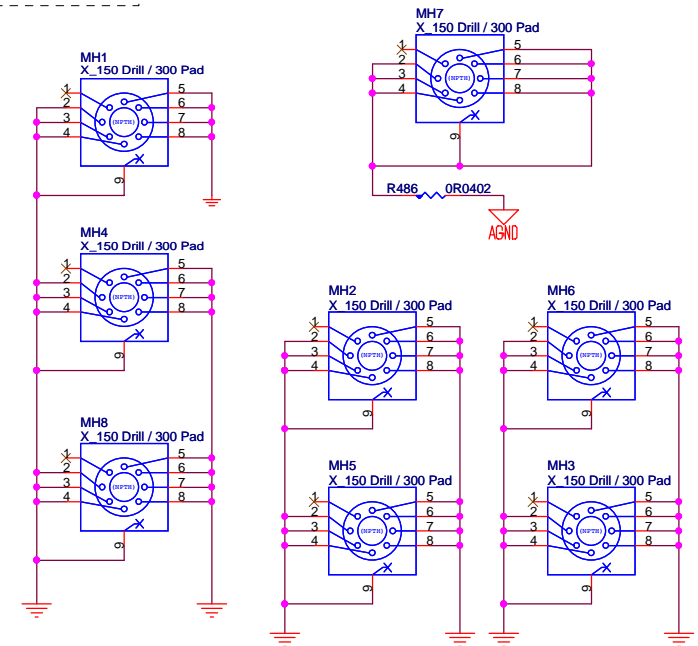
SYS FAN (For Poseidon and Ropros-U use)



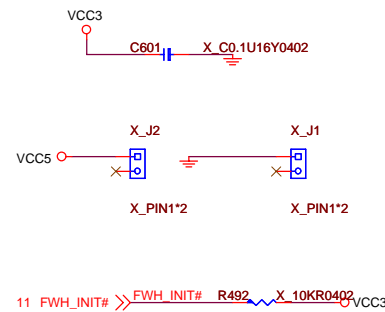
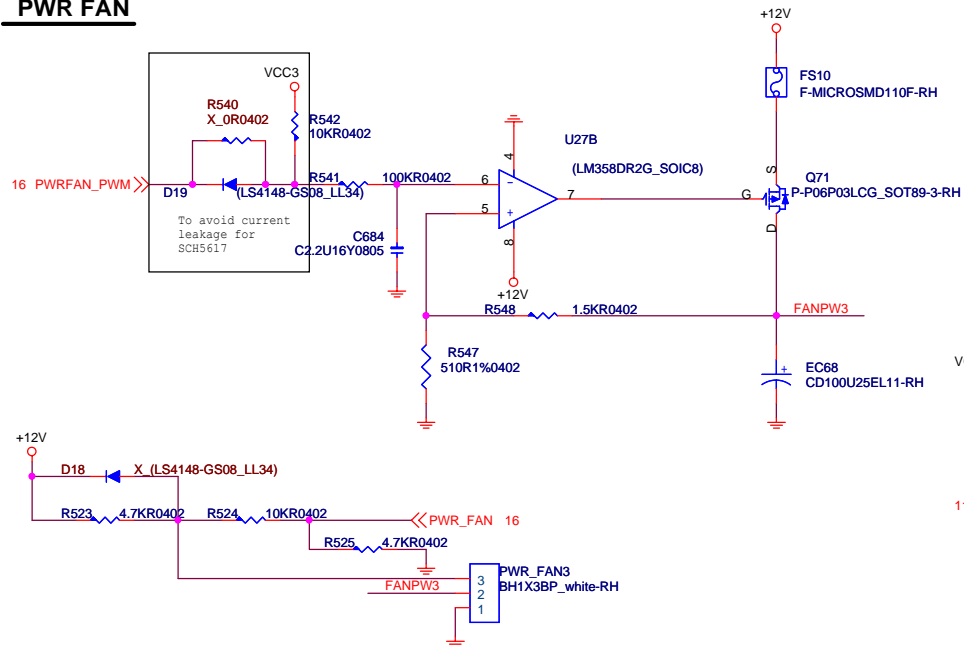
Optical Fiducial Marks




Mounting Holes

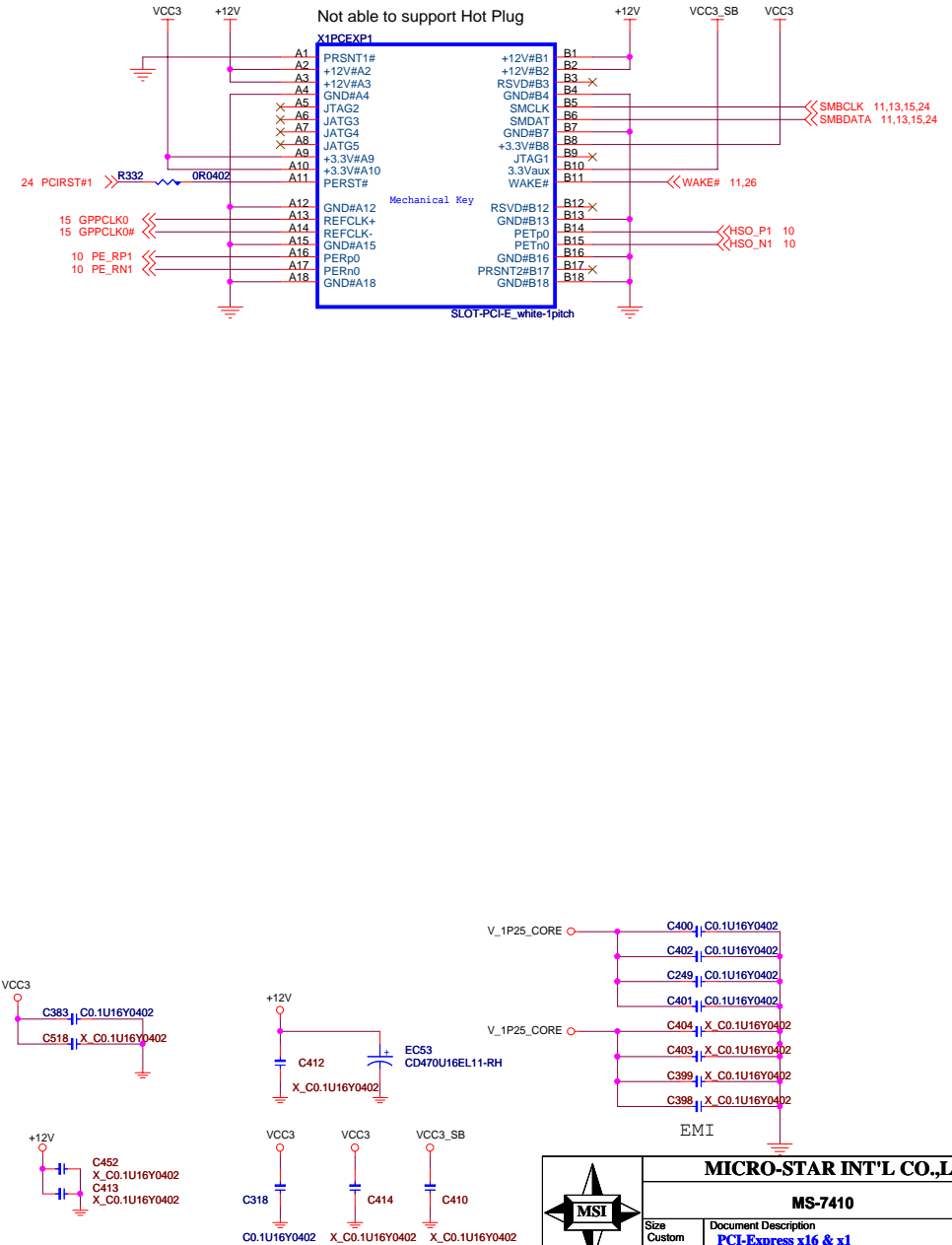
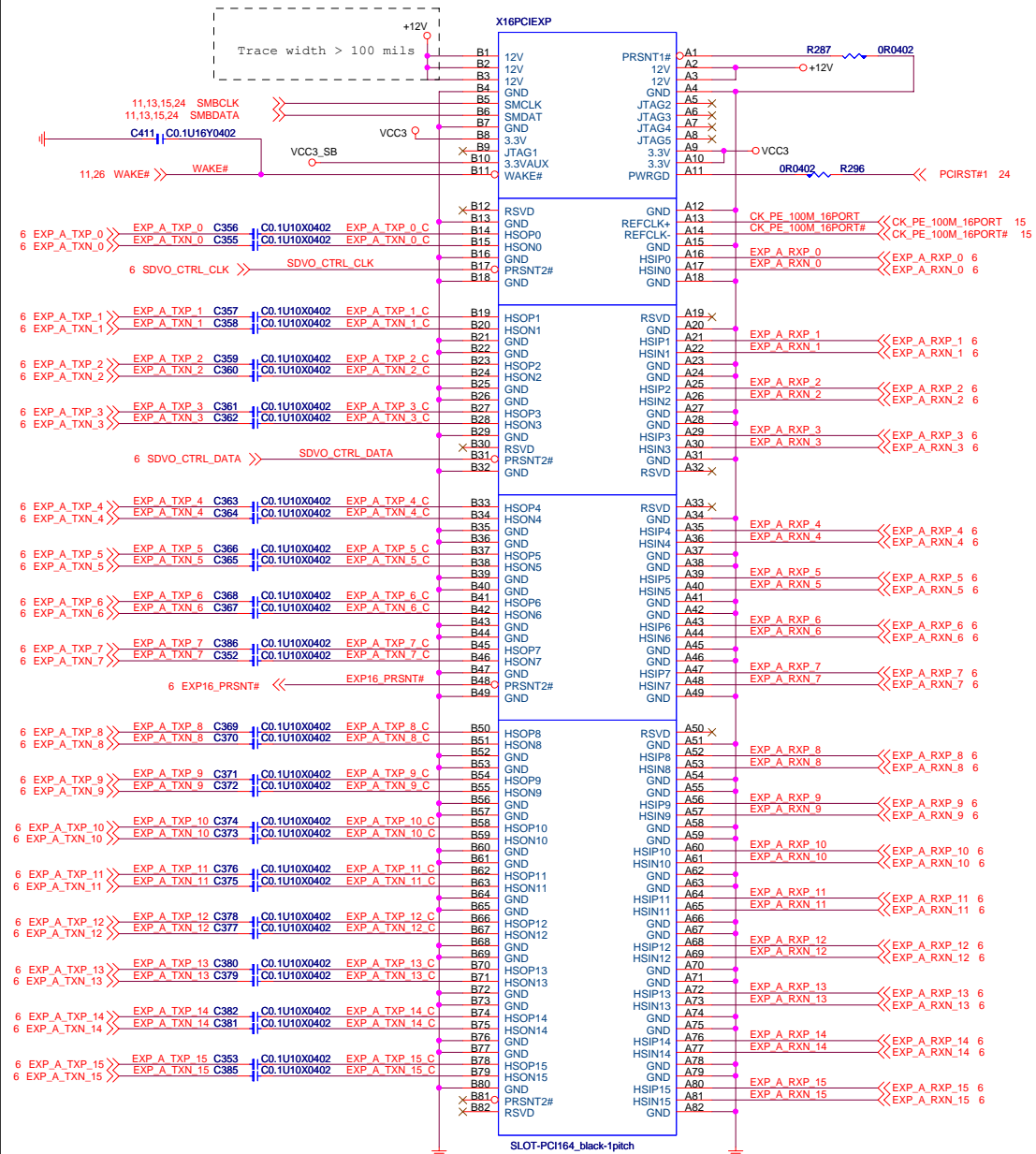


PWR FAN

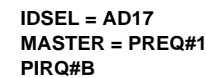
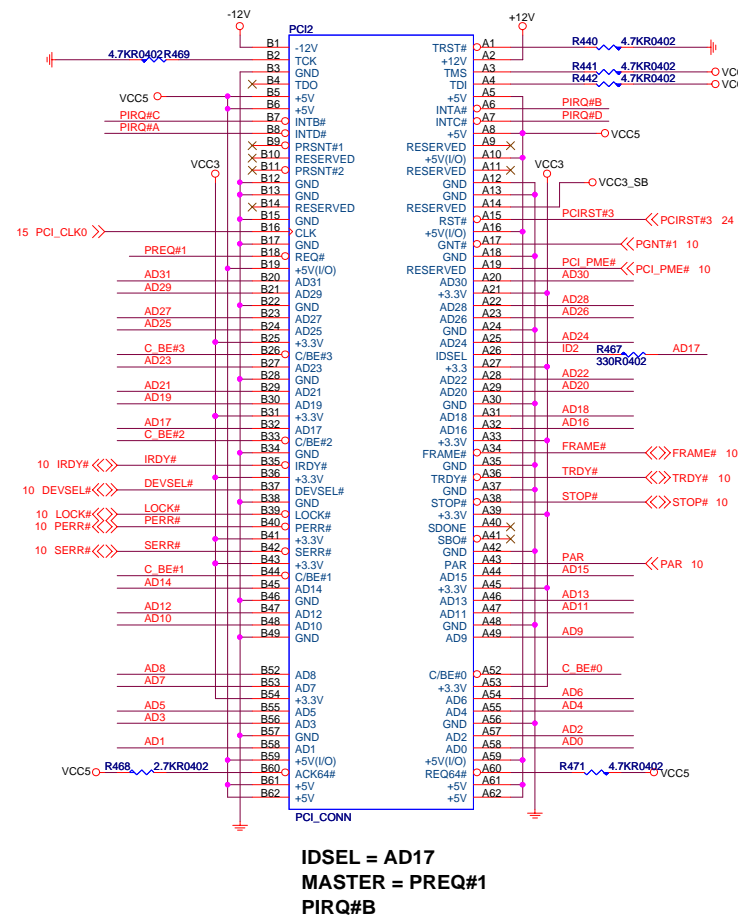


	MICRO-STAR INT'L CO.,LTD		
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	Size B	Document Description CPU/SYS/PWR FAN	Rev 12
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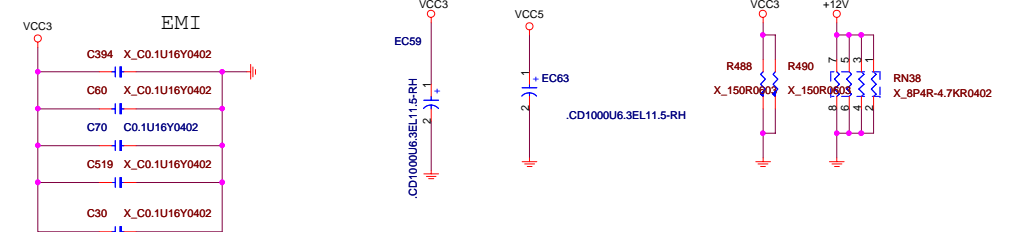
PCI EXPRESS 16-PORT



PCI SLOT 2 (PCI VER: 2.2 COMPLY)



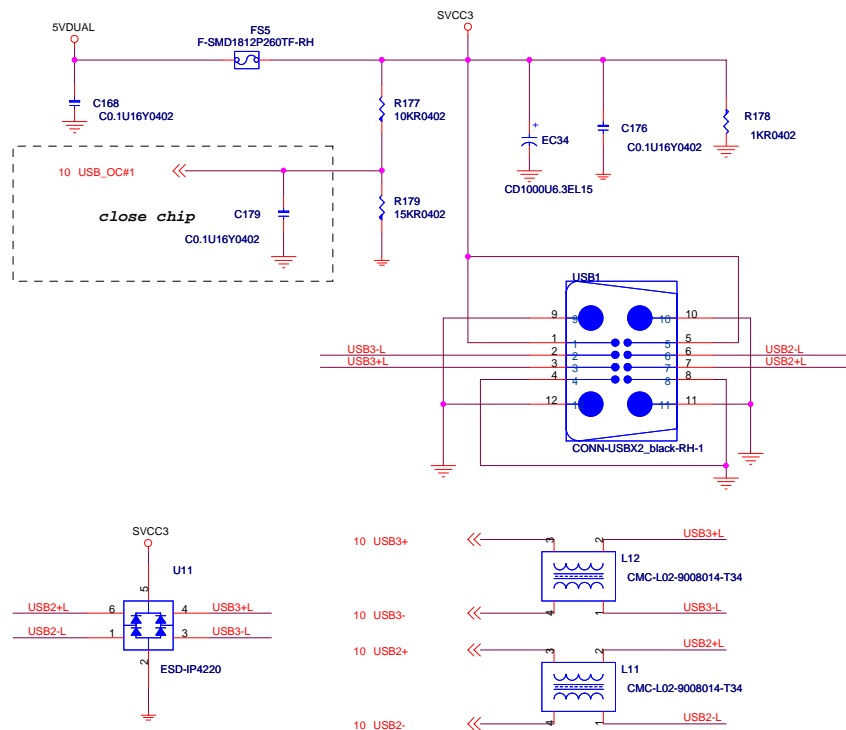
PCI SLOT DECOUPLING CAPACITORS



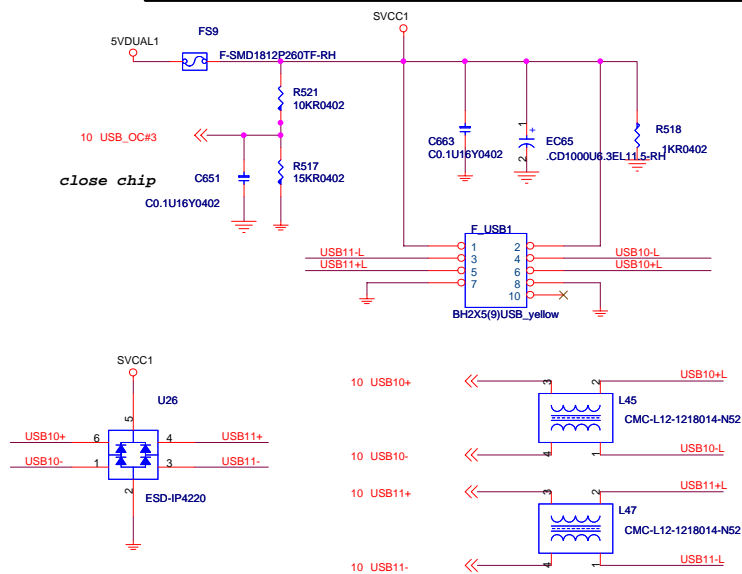
MS-7410

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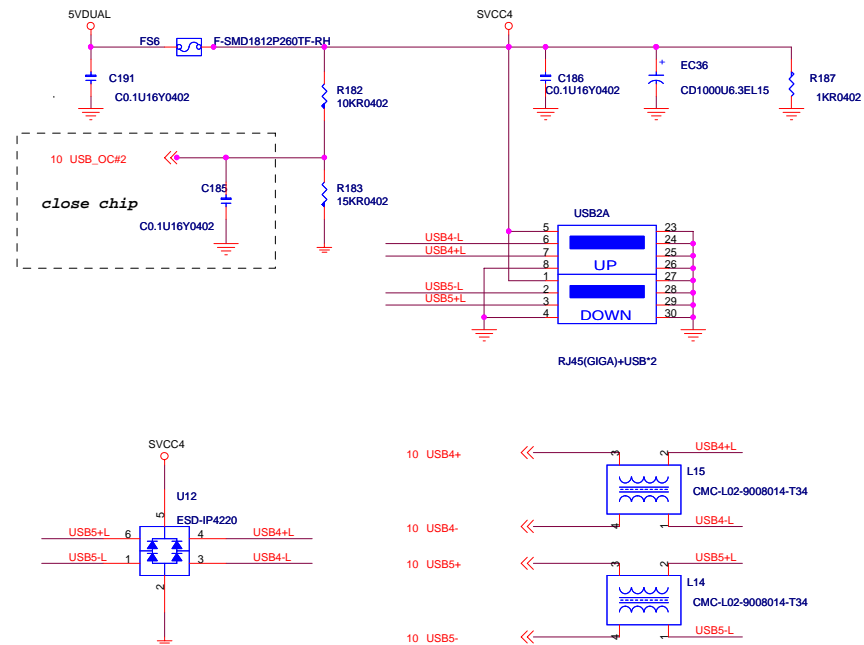
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



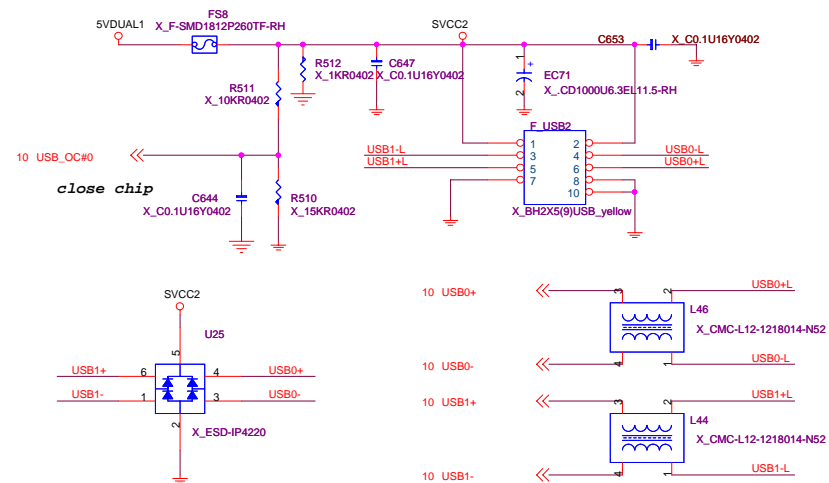
Front USB PORT 10,11 (right angled type) for ROPROS Front USB PORT 10,11 (No housing type) for Poseidon



REAR PANEL USB CONNECTOR FOR USB PORT 4,5



Memory card reader USB CONNECTOR FOR USB PORT 0,1 (FOR ROPROS-VS & Poseidon)

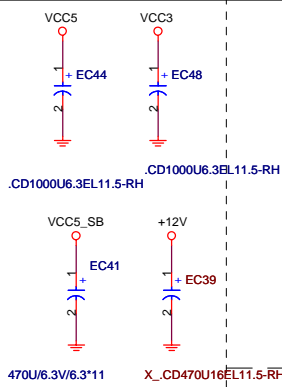
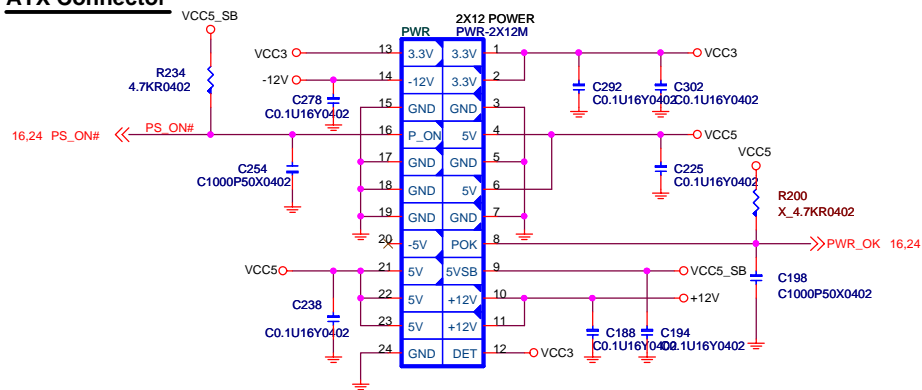


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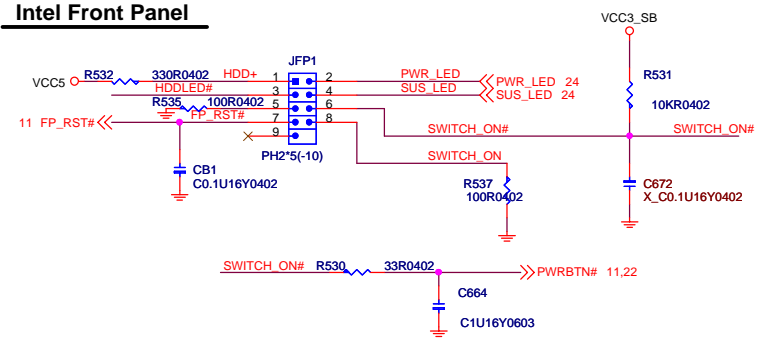
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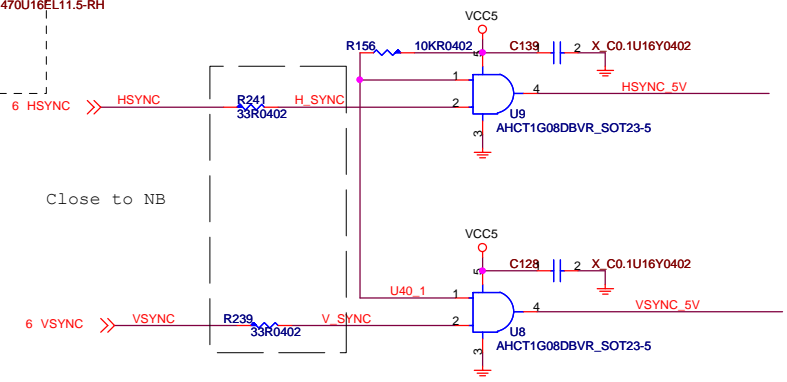
ATX Connector



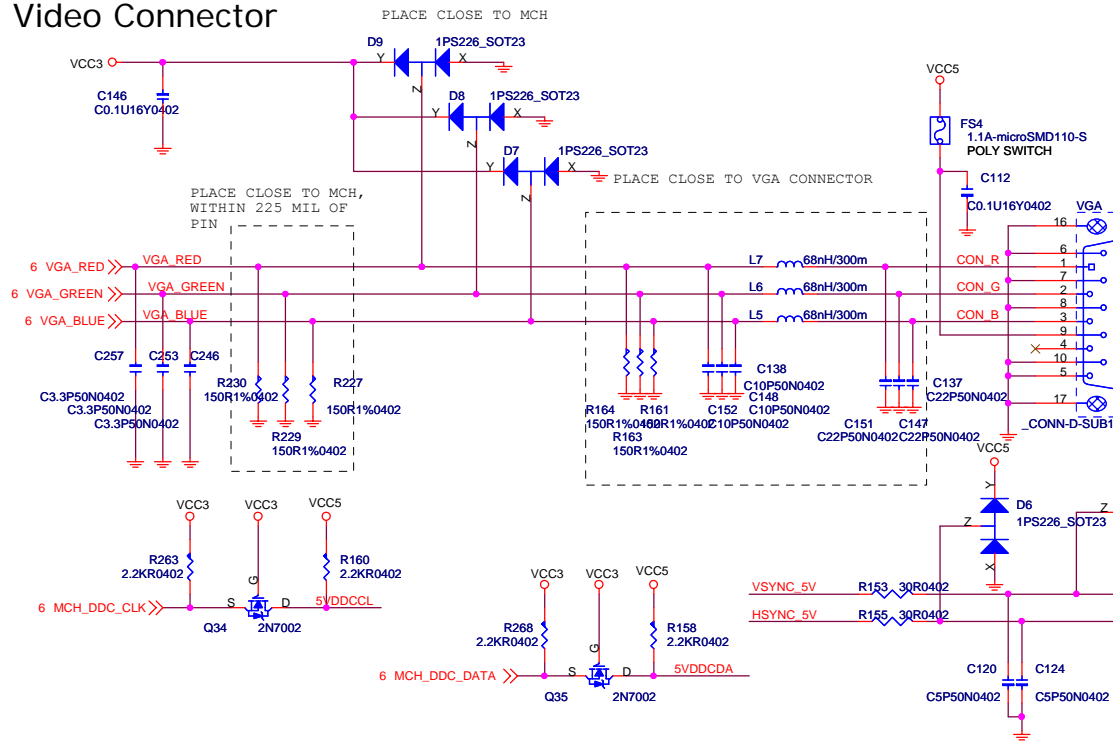
Intel Front Panel



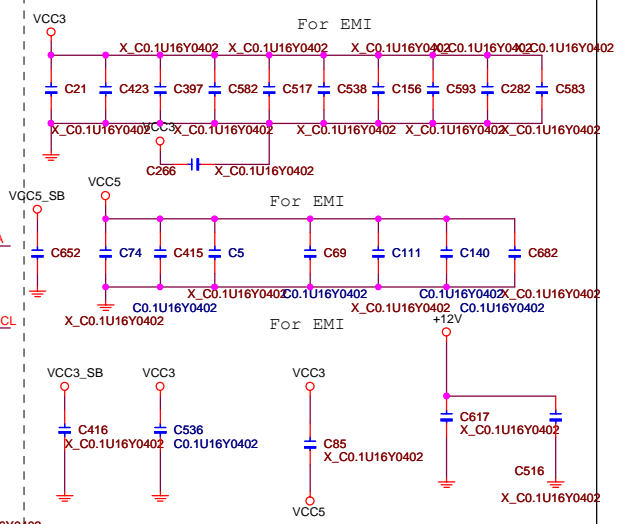
IDE LED



Video Connector

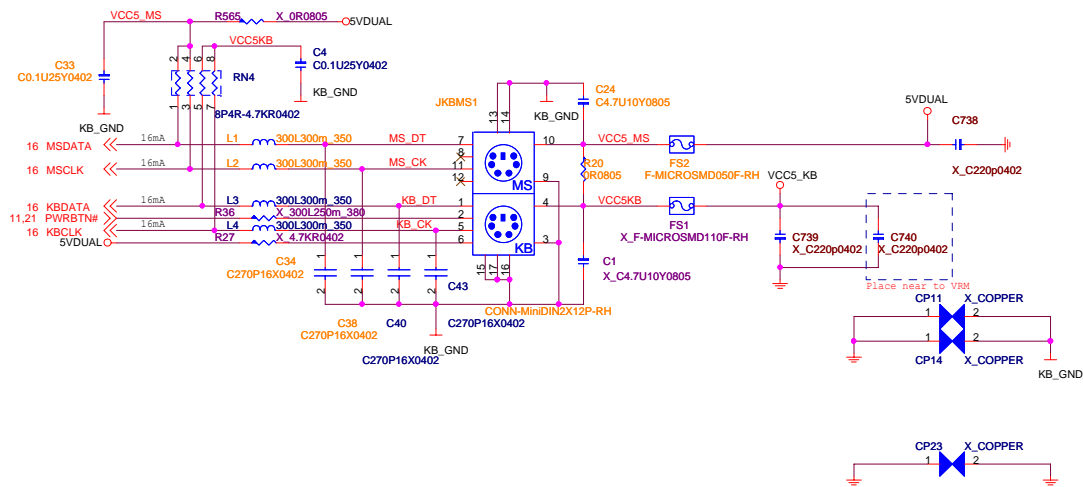


Part Value Selection:	
G:	With 915G option
X:	No Stuff



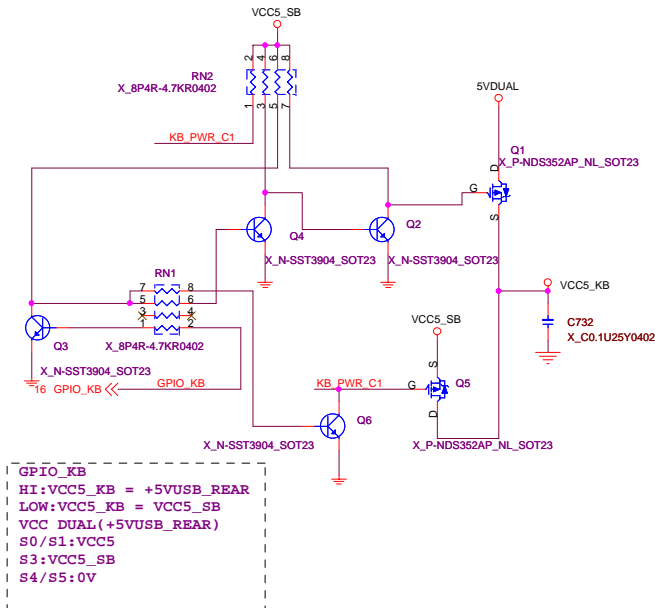
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PS2 KEYBOARD & MOUSE CONNECTOR



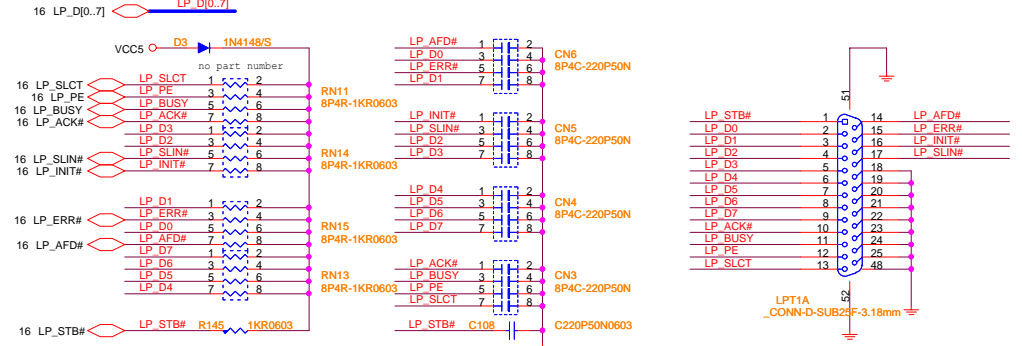
	FS2	R20	C24	L1	L2	C33	C33	C34	C38	FS1	C1	R27	R36
ROPROS-MA	V	V	V	V	V	V	V	V	V	X	X	X	X
ROPROS-VS	X	X	X	X	X	X	X	X	X	V	V	V	V
ROPROS-NECCA	V	V	V	V	V	V	V	V	V	X	X	X	X

K/B Power supply function for ROPROS-VS & Poseidon



GPIO_KB
 HI:VCC5_KB = +5VUSB_REAR
 LOW:VCC5_KB = VCC5_SB
 VCC_DUAL(+5VUSB_REAR)
 S0/S1:VCC5
 S3:VCC5_SB
 S4/S5:0V

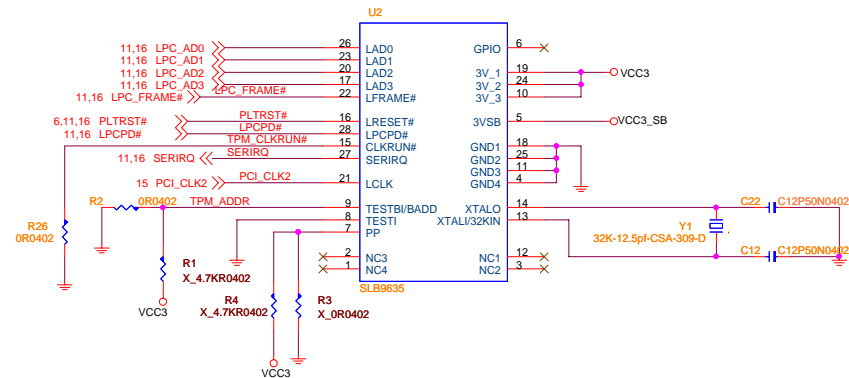
PARALLAL PORT



T.P.M FOR ROPROS-MA

TPM 1.2

IO Address:0x02E



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Voltage Regular Module

N-P0903BDG_TO252
P75N02LDG/TO252
C100U2SP
CD560U4OS-2
1800UF/6.3V
0.25uH/40A
CH-1.1U25A-LF
CD1000U16EL20-2

mosfet/n-channel, P0903BDG, SMT/TO252, Rds(on)=9.5mΩ(10V,25A), Vgs(on)=1~3V, Id=50A, Ciss=1800pF, Qg=50nC, Vds=25V, Vgs=±20V, RoHS compliance

mosfet/n-channel, P75N02LDG, SMT/TO252, Rds(on)=7mΩ(810V, 30A), Vgs(on)=1~3V, Id=75A, Ciss=5000pF, Qg=140nC, Vds=25V, Vgs=±20V, RoHS compliance

ESR<13mΩ, Ripple cur.<2.7A, L=12uA, 105C

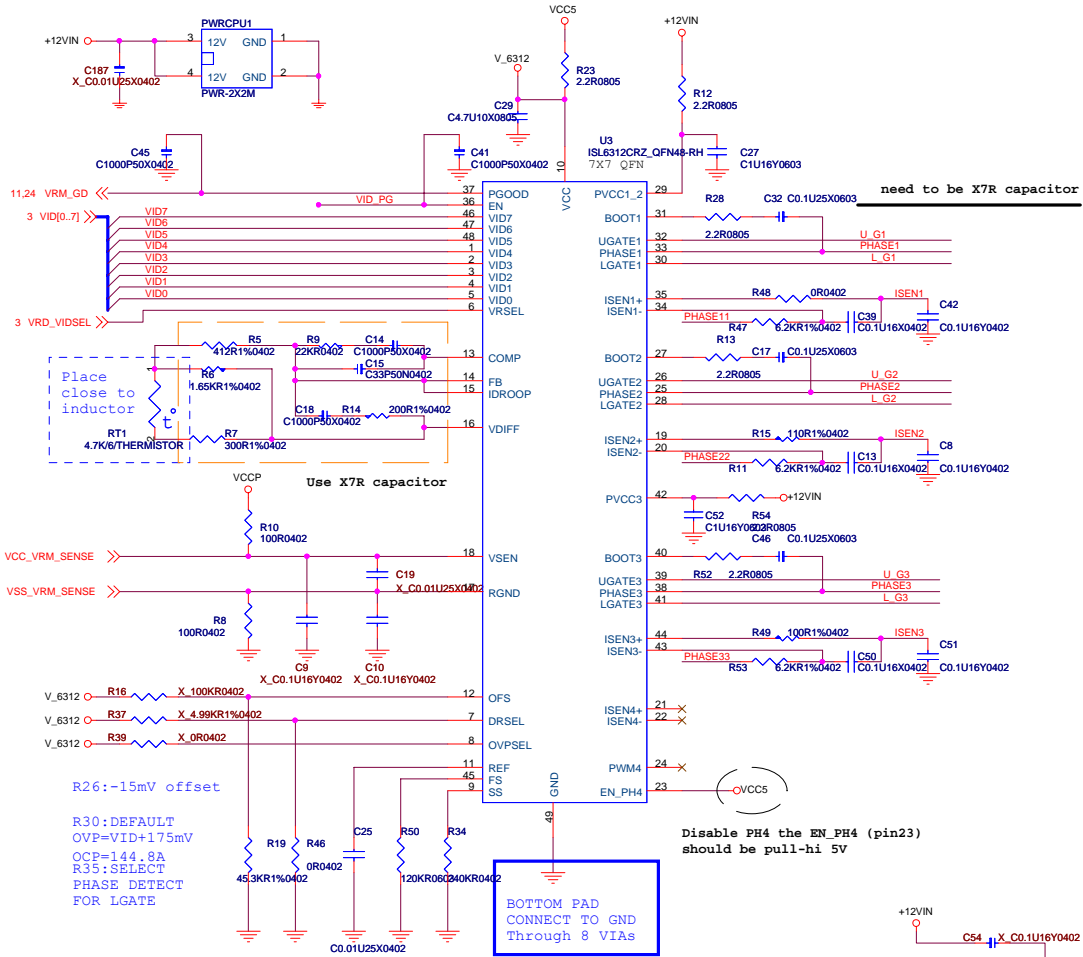
CAP, OS-CON, 560u/4V, Dip-2/8*9/3.5mm, ESR<7mohm, Ripplecur.=6100mA, Lc. <500uA, SPEC series, RoHS compliance

ESR<12mΩ, Ripplecur<2350mA, 105C, longlife change from 2000hrs to 3000hrs ,KZJ series

, IND CHOKE, 0.25uH, 20%, DIP/8.5mm, 40A, 0.6mOhm, , , PEW, FERRITE, SQUARE, RoHS COMPLIANCE

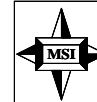
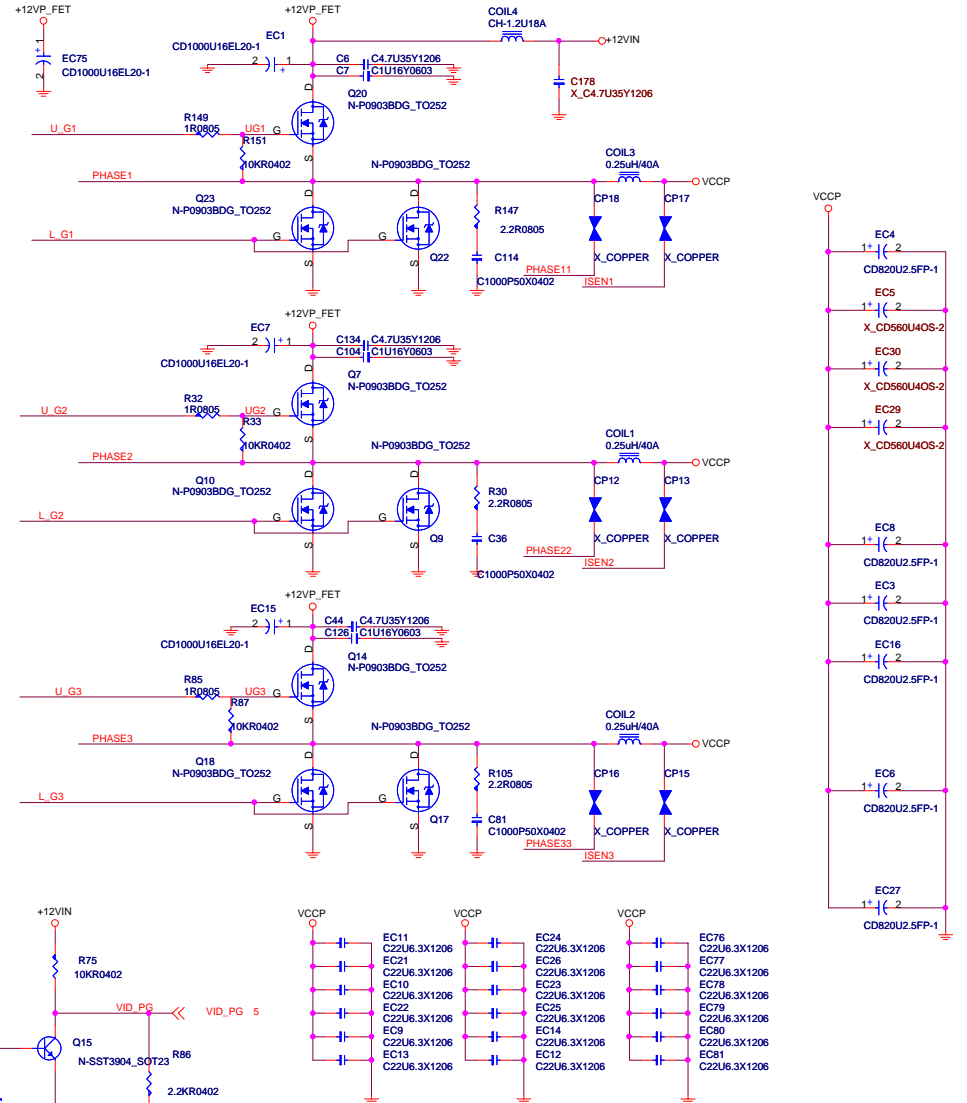
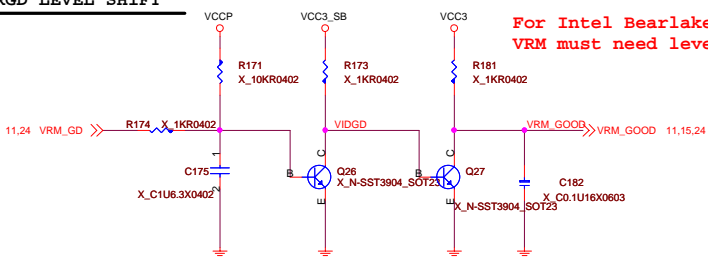
IND CHOKE, 1.1uH, 20%, DIP/9mm, 25A, 1.4mOhm, 5.5T, 0.9mmx3, PEW, IRON, , LEAD FREE

CAP, EL, 1000u, 16V, Dip-8x20/3.5mm, 20%, 12mOhm, 2350mA, 105C, 3000hrs, RoHS COMPLIANCE



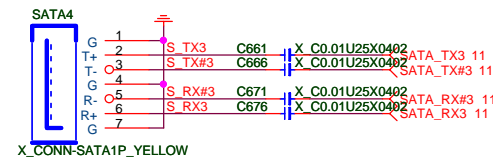
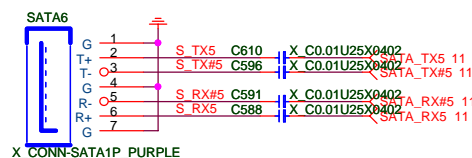
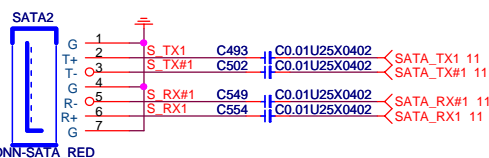
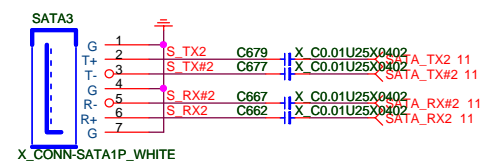
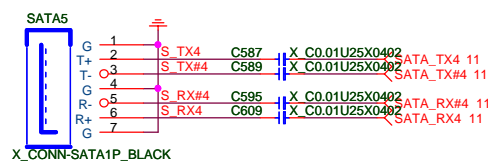
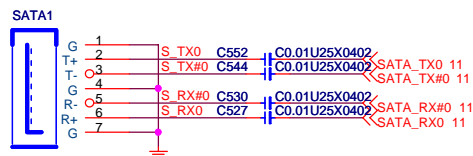
Disable PH4 the EN_PH4 (pin23)
should be pull-hi 5V

For Intel Bearlake Design Guide.
VRM must need level shift



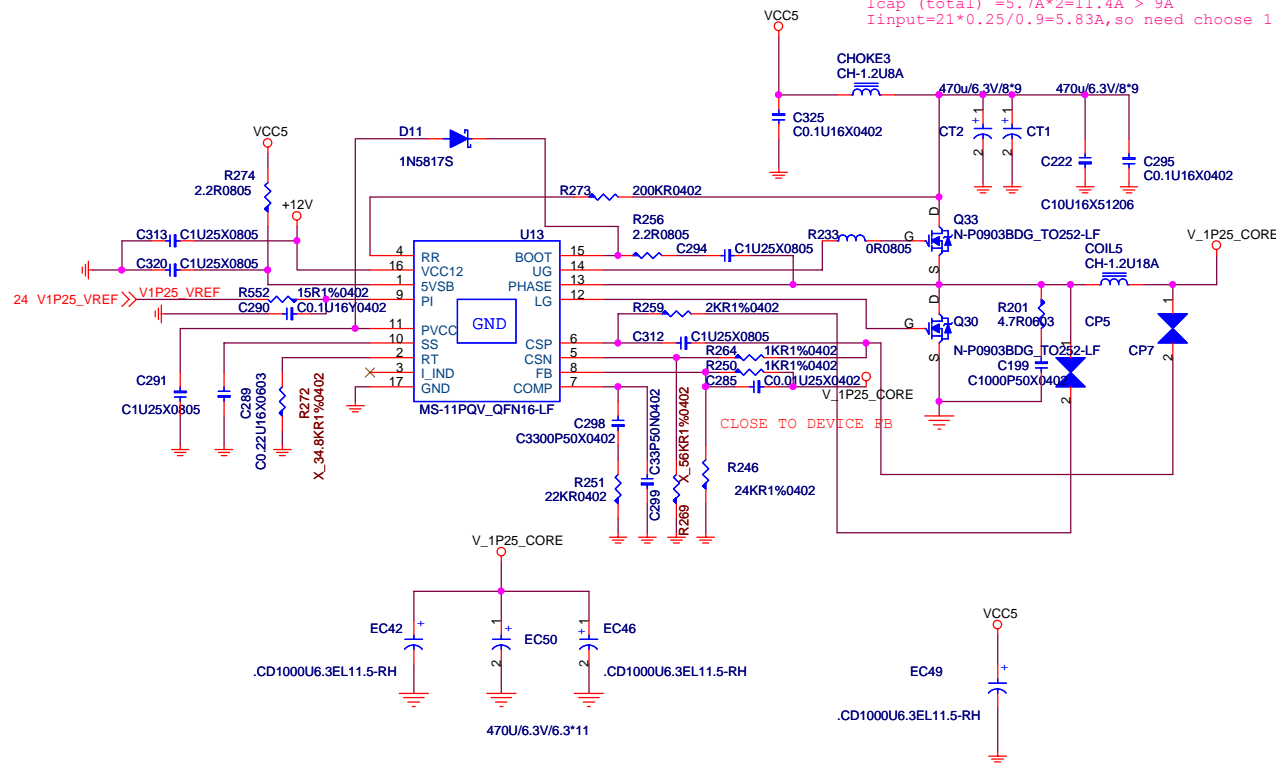
MICRO-STAR INT'L CO.,LTD			
MS-7410			
Size Custom	Document Description VRD11 Intersil 6312 3Phase		Rev 12
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SERIAL ATA CONNECTOR BLOCK SATA1&SATA2 FOR ROPROS-MA/VS USE



GMCH 1.25V POWER (21.3A)

$I_{rms} = 21 \times 0.433 = 9.09A$
 $I_{cap} (total) = 5.7A \times 2 = 11.4A > 9A$
 $I_{input} = 21 \times 0.25 / 0.9 = 5.83A$, so need choose 1.2UH/8A choke



MICRO-STAR INT'L CO.,LTD

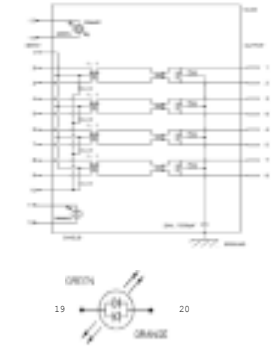
MS-7410

Size	Document Description	Rev
B	SATA&V_1P25_CORE	12
Date:	Tuesday, September 23, 2008	Sheet 25 of 34

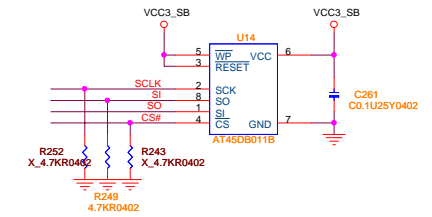
BCM5787M LAN CHIP (ROPROS-MA)

LAN Connector

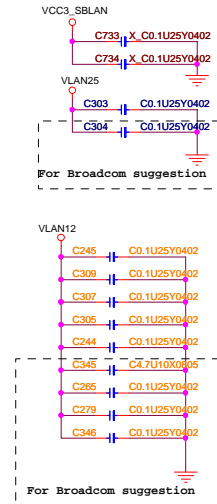
Giga-Lan	
N58-22F0571-F02	
Link	Yellow
Active	Blinking
1000	Orange
100	Green
10	None
21	Yellow
22	Yellow
20	Orange
19	Green



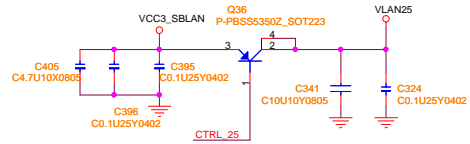
LAN EEPROM



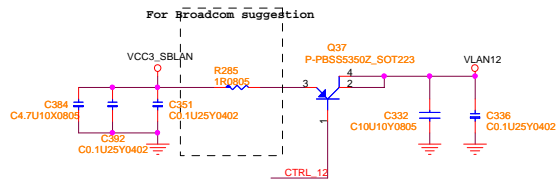
Bypass CAPs



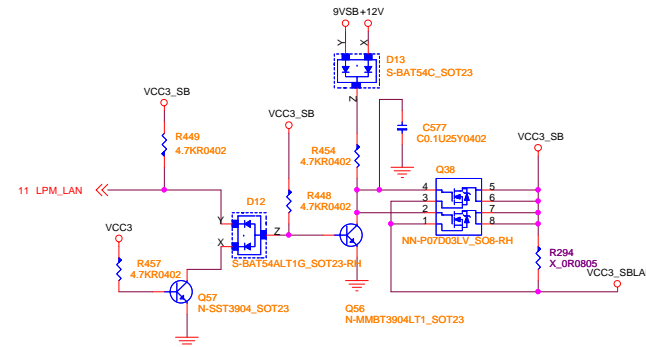
LAN 2.5 POWER (235mA)



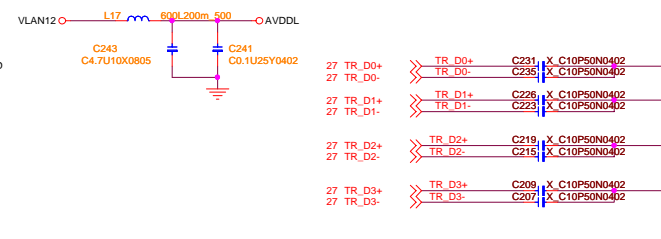
LAN 1.2 POWER (590mA)



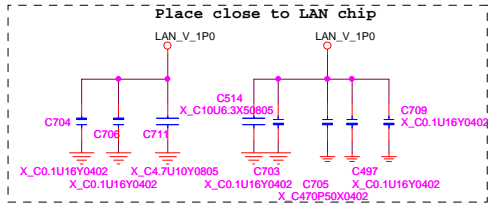
Power control for power consumption



EMI SUGGESTION



LAN - NINEVEH (ROPROS-VS) (Poseidon)



10 GLAN_RXP
10 GLAN_RXN
10 GLAN_TXP
10 GLAN_TXN

GLAN_RXP
GLAN_RXN
GLAN_TXP
GLAN_TXN

C495
C504

X_C0.1U16Y0402
X_C0.1U16Y0402

GLAN_RXP_C
GLAN_RXN_C
GLAN_TXP_C
GLAN_TXN_C

H2
H4
H7
H4

RSVD_J6/NC
RSVD_J7/NC

G7
H7

GLAN_RCOMP_DP
GLAN_RCOMP_DN

E7
E6

RBIAS_P
RBIAS_N/NC

E6
E6

CTRL_10/NC
CTRL_18/NC

C3
B2

THERM_D_P/NC
THERM_D_N/NC

A7
B7

IEEE_TEST_P/NC
IEEE_TEST_N/NC

G1
H1

JTAG_TCK/ISOL_TCK
JTAG_TDI/ISOL_TDI

G3
G3

JTAG_TDO/TOUT
JTAG_TMS/ISOL_EXEC

G3
G3

VSSA_VSS
VSSA_VSS

VSSA_VSS
VSSA_VSS

VSSA_VSS
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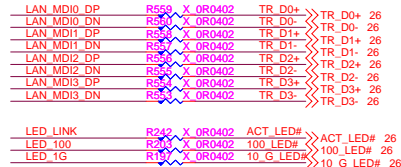
VSSA_VSS
VSSA_VSS

VSSA_VSS
VSSA_VSS

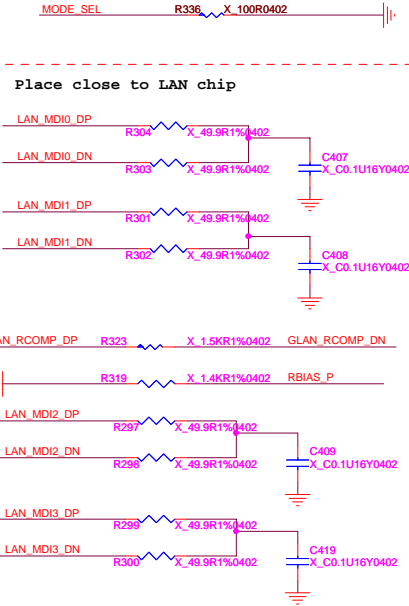
VSSA_VSS
VSSA_VSS

Nineveh 8256DC

LAN CONNECTOR

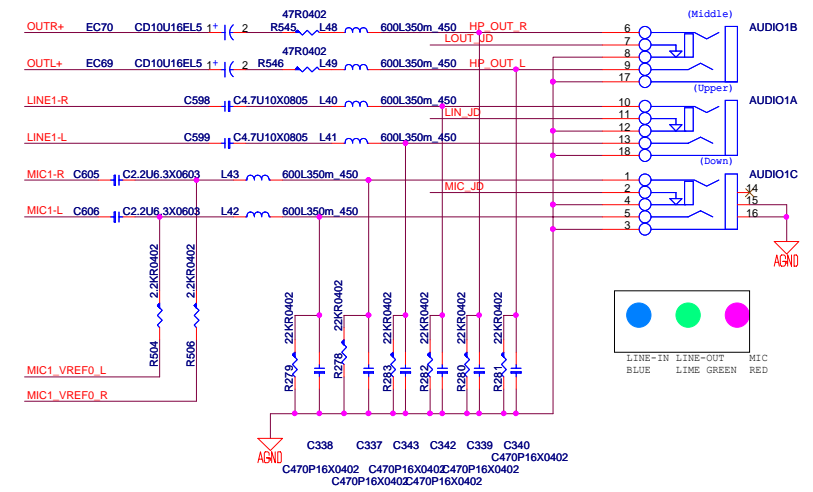
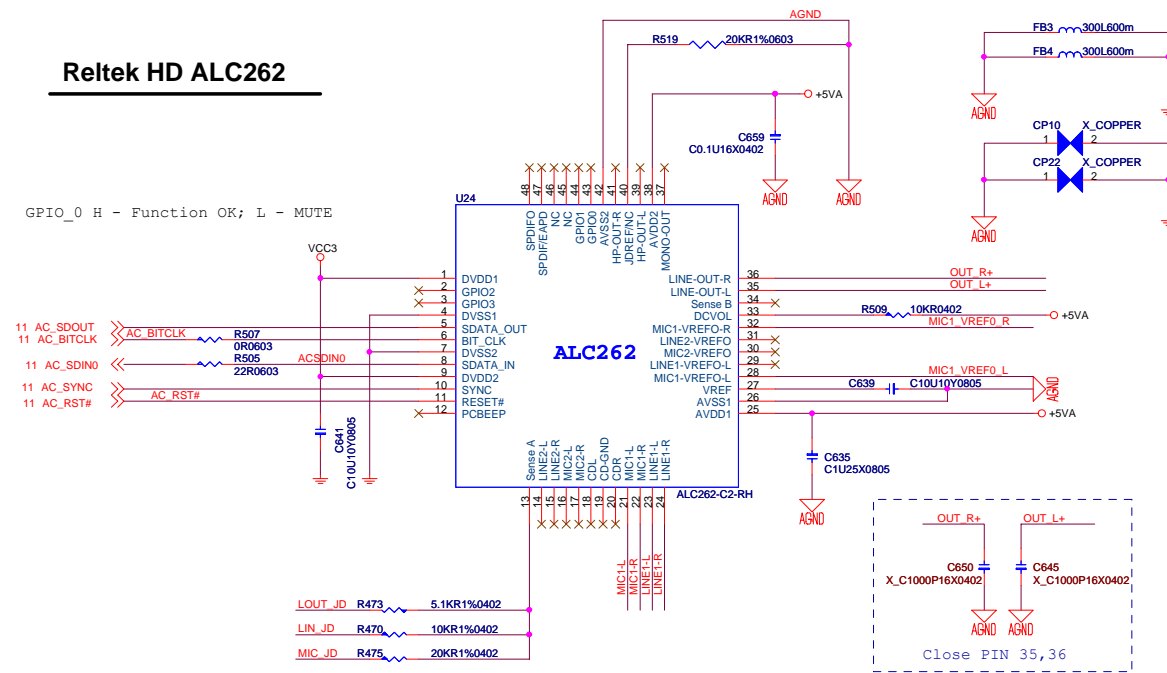


ACT_LED	Link_LED
S0: LOW	S0: LOW
S1/S3/S4/S5: HIGH	S5: HIGH
	S1/S3/S4: WOL EN-->LOW WOL DIS-->HIGH

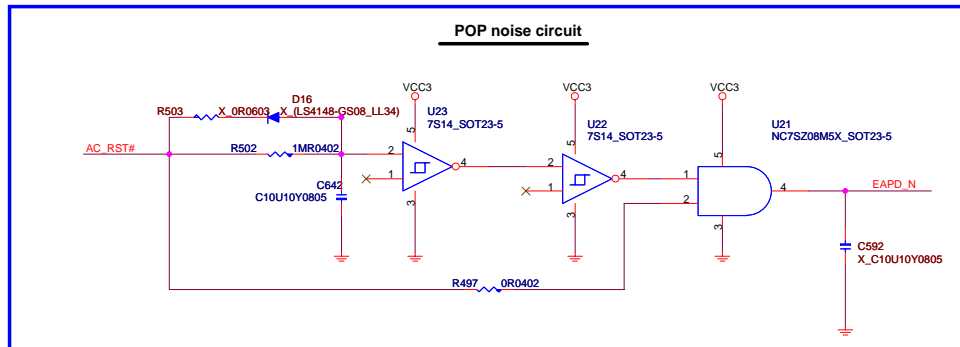


Reltek HD ALC262

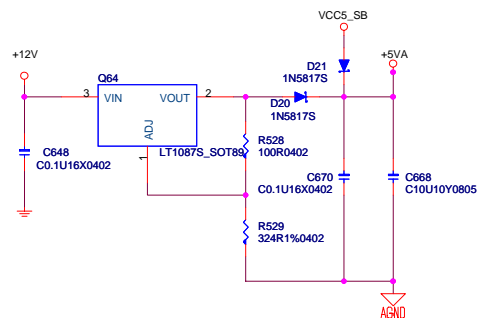
GPIO_0 H - Function OK; L - MUTE



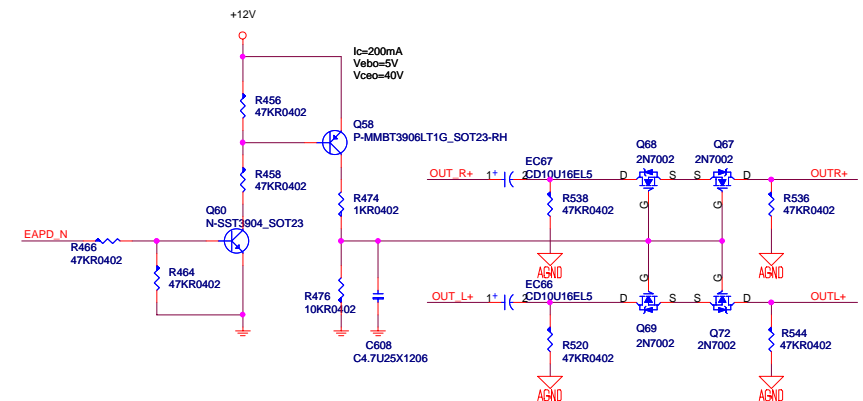
08/01 UPDATE



AUDIO CODE REGULATORS



Smooth pop noise circuit for Line-out



MICRO-STAR INT'L CO.,LTD

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ICH9

GPIO	Alt Func	Pin	I/O/NC	Power	PU	Tol	Default	Signal Name or condition
GPIO[0]	ATADET0	N7	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[1]	PULL HIGH	AK21	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[2]	PIRQ#E	K6	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 8.2K
GPIO[3]	PIRQ#F	L7	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 8.2K
GPIO[4]	PIRQ#G	F2	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 8.2K
GPIO[5]	PIRQ#H	G2	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 8.2K
GPIO[6]	PULL HIGH	AH22	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[7]	PULL HIGH	AK23	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[8]	ICH GP8 PU	A20	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH 10K
GPIO[9]	NC	A18	NC	Vcc3	N	3.3	WOL EN	NC
GPIO[10]	ICH GP10 PU	C17	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH 10K
GPIO[11]	SMB ALERT#	C16	I/O	Vcc3SB	Y	3.3	SMB ALERT#	PULL HIGH 10K
GPIO[12]	SIO SMI#	A8	I/O	Vcc3SB	Y	3.3	OUTPUT	PULL HIGH 10K with SIO SMI#
GPIO[13]	SIO PME#	A19	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH 10K with SIO PME#
GPIO[14]	CLR PW	A9	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH 10K
GPIO[15]	NC	C15	NC	Vcc3SB	N	3.3	STP PCI#	NC
GPIO[16]	NC	M2	NC	Vcc3	N	3.3	OUTPUT	NC
GPIO[17]	PULL HIGH	AH21	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[18]	NC	K1	NC	Vcc3	N	3.3	OUTPUT	NC
GPIO[19]	SATA1GP PU	AE20	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[20]	NC	AF5	NC	Vcc3	N	3.3	OUTPUT	TP15 (As PWROK)
GPIO[21]	SATA0GP PU	AK25	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[22]	ICH SGP22 PU	AJ24	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[23]	LDRQ 1#	J3	I/O	Vcc3	Y	3.3	LDRQ 1#	PULL HIGH 10K
GPIO[24]	LPM LAN	A14	I/O	Vcc3SB	Y	3.3	OUTPUT	LPM LAN
GPIO[25]	NC	B18	NC	Vcc3SB	N	3.3	STP CPU#	NC
GPIO[26]	NC	C11	NC	Vcc3SB	N	3.3	S4 STATE#	NC
GPIO[27]	NC	A11	NC	Vcc3SB	N	3.3	OUTPUT	NC
GPIO[28]	NC	G18	NC	Vcc3SB	N	3.3	OUTPUT	NC
GPIO[29]	USB OC#2	N1	I/O	Vcc3SB	Y	3.3	OC#5	USB OC#2
GPIO[30]	USB OC#3	N5	I/O	Vcc3SB	Y	3.3	OC#6	USB OC#3
GPIO[31]	USB OC#3	M1	I/O	Vcc3SB	Y	3.3	OC#7	USB OC#3
GPIO[32]	SPI WP#	K2	I/O	Vcc3	Y	3.3	OUTPUT	PULL HIGH 2.2K with SPI_WP#
GPIO[33]	SPI HOLD GPO#	AF6	I/O	Vcc3	Y	3.3	OUTPUT	PULL HIGH 10K
GPIO[34]	NC	AH5	NC	Vcc3	N	3.3	OUTPUT	NC
GPIO[35]	NC	L1	NC	Vcc3	N	3.3	OUTPUT	NC
GPIO[36]	SATA2GP PU	AE21	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[37]	SATA3GP PU	AE22	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[38]	ICH SGP38 PU	AK24	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[39]	ICH SGP39 PD	AH23	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[40]	USB OC#0	N3	I/O	Vcc3SB	Y	3.3	OC#1	USB OC#0
GPIO[41]	USB OC#1	P7	I/O	Vcc3SB	Y	3.3	OC#2	USB OC#1
GPIO[42]	USB OC#1	R7	I/O	Vcc3SB	Y	3.3	OC#3	USB OC#1
GPIO[43]	USB OC#2	N2	I/O	Vcc3SB	Y	3.3	OC#4	USB OC#2
GPIO[44]	USB OC#3	P3	I/O	Vcc3SB	Y	3.3	OC#8	USB OC#3
GPIO[45]	USB OC#3	R6	I/O	Vcc3SB	Y	3.3	OC#9	USB OC#3
GPIO[46]	USB OC#3	T7	I/O	Vcc3SB	Y	3.3	OC#10	USB OC#3
GPIO[47]	USB OC#3	P1	I/O	Vcc3SB	Y	3.3	OC#11	USB OC#3
GPIO[48]	ICH SGP48 PD	AD20	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[49]	DMI STRAP	AJ25	I/O	Vcc3	Y	3.3	OUTPUT	PULL LOW 2.2K
GPIO[50]	PREQ#1	G13	I/O	Vcc5	Y	5.5	PREQ#1	PULL HIGH 2.7K with PREQ#1
GPIO[51]	PGNT#1	A7	I/O	Vcc3	Y	3.3	PGNT#1	PGNT#1
GPIO[52]	PREQ#2	F13	I/O	Vcc5	Y	5.5	PREQ#2	PULL HIGH 2.7K with PREQ#2
GPIO[53]	PGNT#2	C7	I/O	Vcc3	Y	3.3	PGNT#2	STRAP PIN
GPIO[54]	PREQ#3	G8	I/O	Vcc5	Y	5.5	PREQ#3	PULL HIGH 2.7K with PREQ#3
GPIO[55]	PGNT#3	F7	I/O	Vcc3	Y	3.3	PGNT#3	STRAP PIN
GPIO[56]	ICH GP56 PU	F16	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH 10K
GPIO[57]	LAN DISABLE	C12	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH 10K with LAN DISABLE
GPIO[58]	SPI CS1#	F23	I/O	Vcc3SB	Y	3.3	INPUT	SPI CS1# (No any connect)
GPIO[59]	USB OC#0	P5	I/O	Vcc3SB	Y	3.3	OC#0	USB OC#0
GPIO[60]	LINK ALERT#	F18	I/O	Vcc3SB	Y	3.3	LINK_ALERT#	PULL HIGH 10K

SIO SCH5617

PIN NAME	PIN#	USAGE	Input/Output
GP76	53	GPIO_KB	OUTPUT
GP42	27	SIO_SMI#	OUTPUT
GP41	77	SIO_PME#	OUTPUT

PCI Config.

DEVICE	MCP1 INT Pin	REQ# /GNT#	IDSEL	CLOCK
PCI1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK0
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A2H	MCLK_A1/MCLK_A#3 MCLK_A2/MCLK_A#4 MCLK_A2/MCLK_A#5
DIMM 3	A4H	MCLK_B0/MCLK_B#0 MCLK_B2/MCLK_B#1 MCLK_B1/MCLK_B#2
DIMM 4	A6H	MCLK_B0/MCLK_B#3 MCLK_B1/MCLK_B#4 MCLK_B2/MCLK_B#5

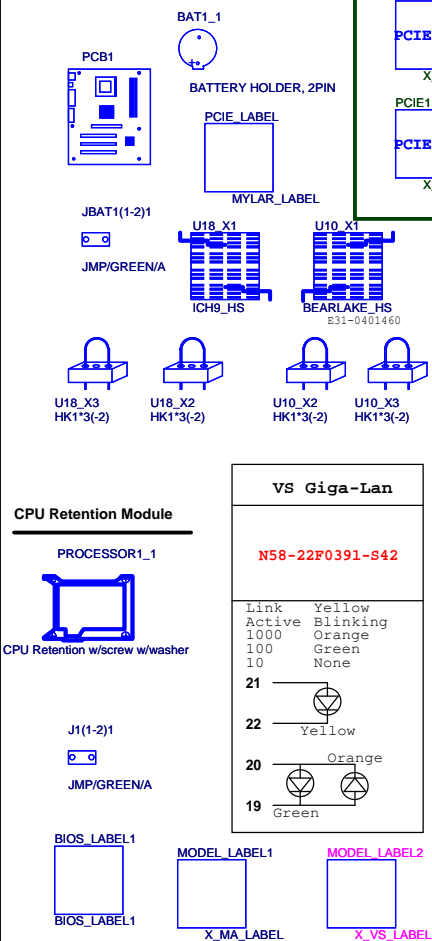
JUMPER SETTING

JBAT1	(1-2) NORMAL	(2-3) CLEAR
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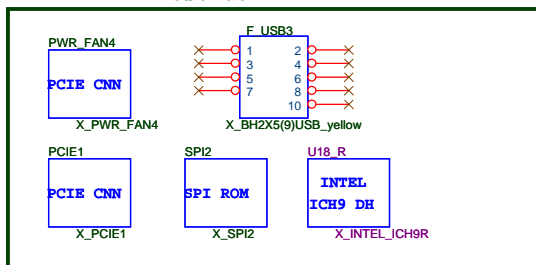


MICRO-STAR INT'L CO.,LTD			
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Size Custom	Document Description GPIO & Jumper setting		Rev 12
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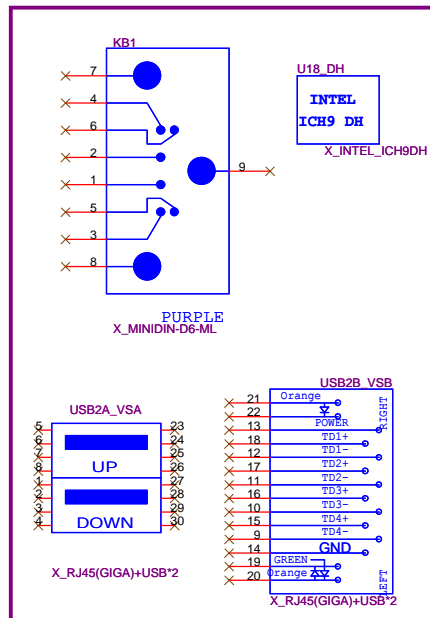
MANUAL PART



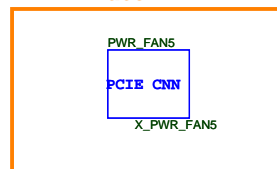
Poseidon



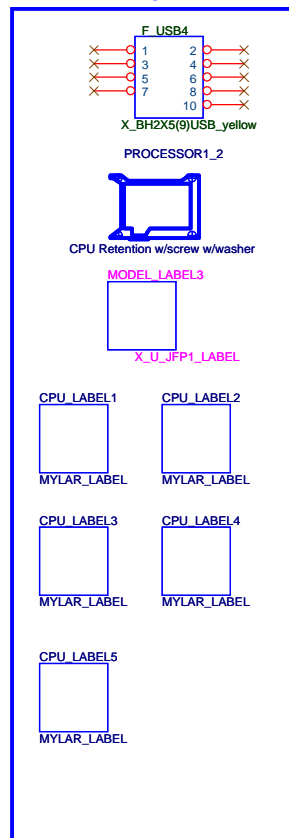
REPROS-VS & Poseidon



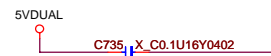
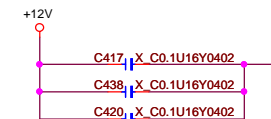
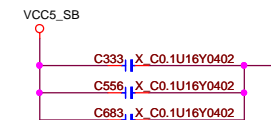
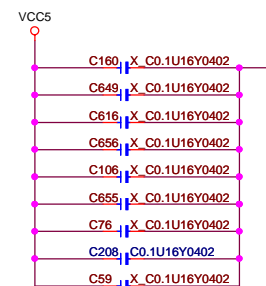
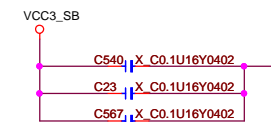
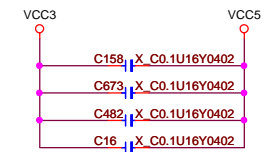
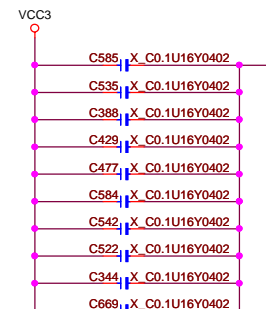
Mate



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EMI SUGGESTION



Model option table

Model type	Function		
ROPROS-MA	INTEL G33 + ICH9 + Broadcom Giga Lan		
ROPROS-VS	INTEL G33 + ICH9DH + Intel 82566 Giga Lan + 2 SATA + Right engle USB		
Poseidon	INTEL G33 + ICH9R + Intel 82566 Giga Lan + 6 SATA + No Housing USB		

BOM Config

ERP BOM No.

LGA775 CPU		
0.8375V - 1.6000V Core	-	100A
1.2V FSB Vtt	-	5.3A

Bearlake-G (G33)		
1.2V FSB_VTT	-	1.3 A
1.25V Core	-	18.8A
1.25V DMI/PCI Exp.	-	2.5 A
1.8V VCC_DDR (S0,S1)	-	3.73A
1.8V VCC_SMCLK	-	TBD
3.3V VCCA_DAC	-	66 mA
3.3V VCC33	-	15.8mA
1.25V Vcc CL	-	4.24A

ICH9		
1.05V Core	-	1.17A
1.25V DMI	-	40 mA
1.2V FSB_VTT	-	14 mA
1.5V_A USB/SATA	-	1.12A
1.5V_B PCI Exp.	-	0.77A
VCCRTC	-	6 uA
3.3V CL	-	12 mA
1.5V GbE LAN	-	74 mA
3.3V 10/100 LAN	-	12 mA
3.3V GbE LAN	-	1 mA
3.3V SusHDA	-	4 mA
3.3V HDA	-	24 mA

3.3V CL	-	12 mA
1.5V GbE LAN	-	74 mA
3.3V 10/100 LAN	-	12 mA
3.3V GbE LAN	-	1 mA
3.3V SusHDA	-	4 mA
3.3V HDA	-	24 mA

HD Audio ALC662		
3.3V AUDIO	-	40mA
5V AUDIO	-	200mA

CK505		
3.3V VDD 48/PCI/REF	-	TBDA
0.3V - 1V CPU/SRC/DOT/PLL	-	TBDA

BCM5786		
3.3V_SB I/O & LED	-	15.5mA
2.5V ANALOG	-	0.418A

ISL6312		
VCCP	VRM 11	
0.8375V-1.6000V	85A	
3-Phase Switch		

W83310DS		
VTT_DDR		
0.9V Linear	2A	

MS11+ Regulator		
VCC_DDR		
1.8V PWM	15A	

MS7 Regulator		
V_1P25_CORE		
1.25V PWM	21.34A	
V_1P25_CL		
1.25V Linear	4.24A	
V_FSB_VTT		
1.2V Linear	6.2A	
V_1P5_ICH	2A	
1.5V Linear		
V_1P05_ICH		
1.05V Linear	2 A	
VCC3_SB		
3.3V Linear	1.5A	
5V Switch	5A	
5VSB Switch	500mA	
5V Switch	15A	
5VSB Switch	500mA	

DDRII x4 & TERMINATOR		
0.9V VTT_DDR	-	1.2A
1.8V VCC_DDR (S0,S1)	-	9.4A
1.8V VCC_DDR (S3)	-	400mA

PCI Express x16 slot		
+12V	-	5.5 A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

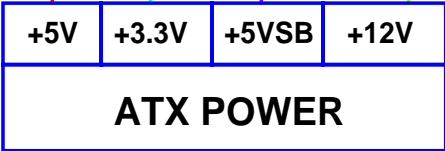
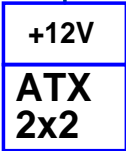
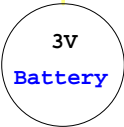
PCI slot x1		
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	7.6A
+5V	-	5.0A
+12V	-	0.5A

PCI Express x 1 slot *2		
+12V	-	0.5 A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

USB x12		
+5V (S0,S1)	-	6.0A
+5V (S3)	-	20mA

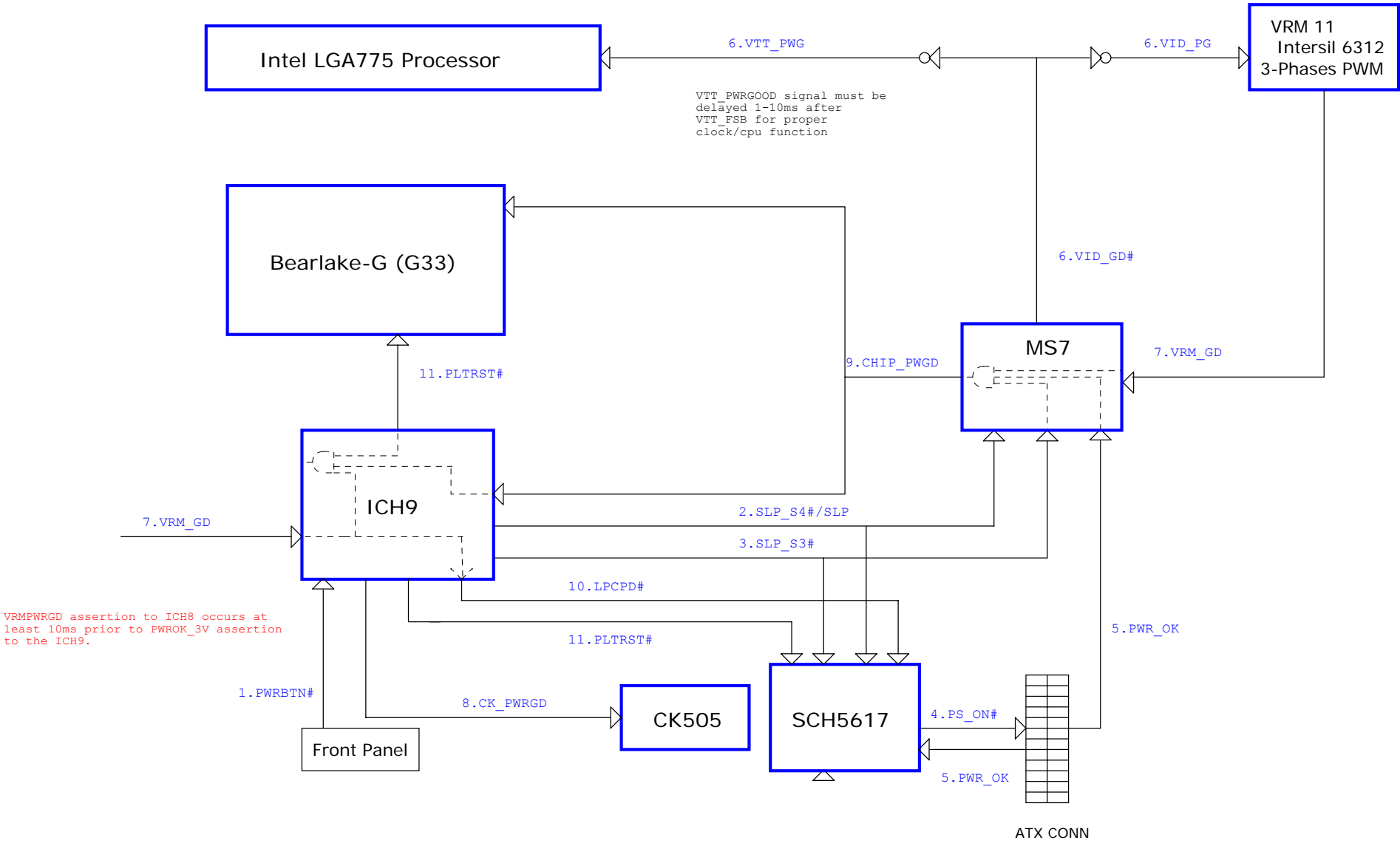
PS2		
+5V (S0,S1)	-	345mA
+5V (S3)	-	2.0mA

5VAUD	5V	500mA
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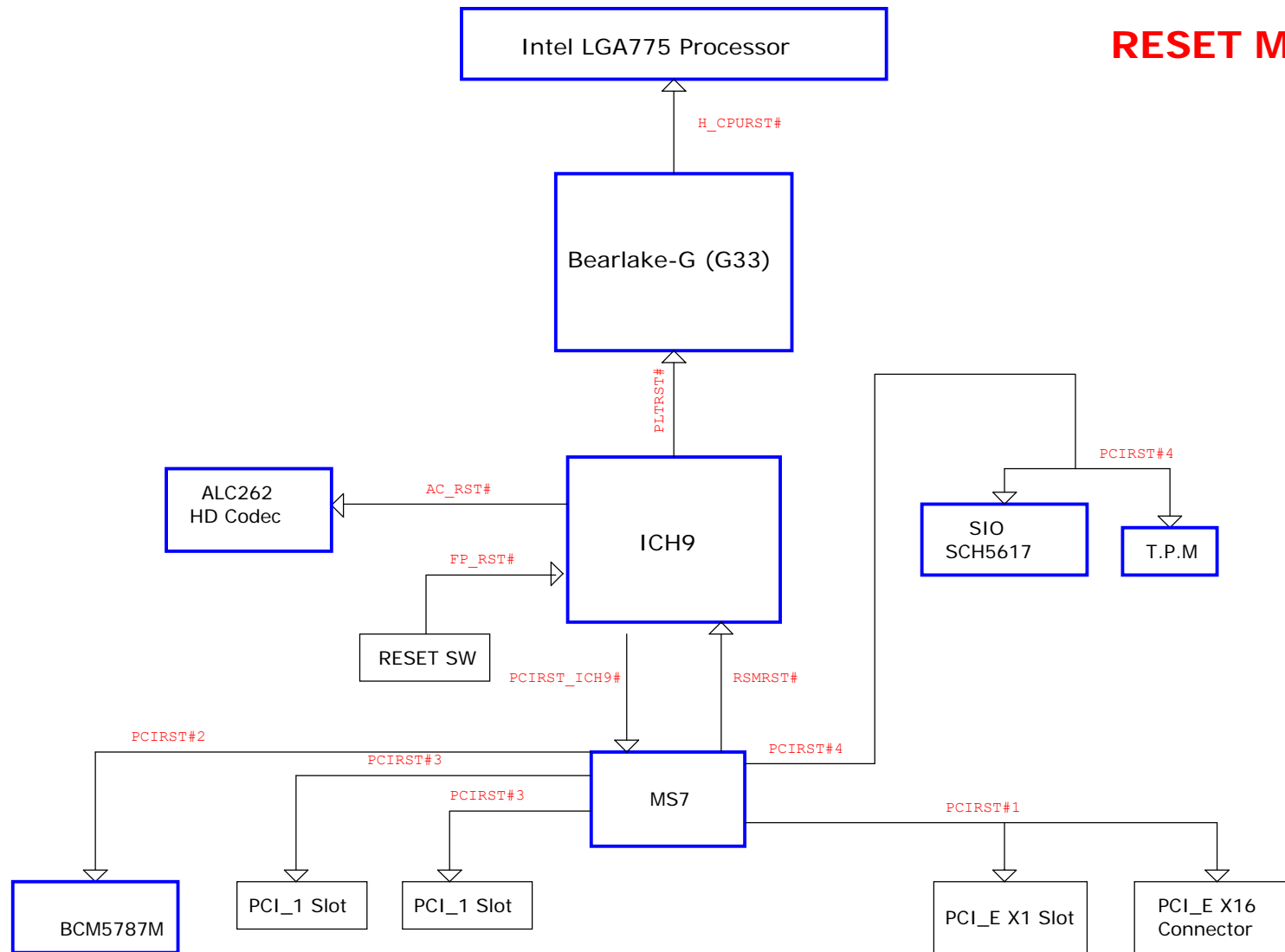


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PWROK MAP



RESET MAP



MICRO-STAR INT'L CO.,LTD

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Change Note

Ver:0A

2007/09/06

- 1.PAGE 4:Add R561 C721 Q73 for VTT SEL control circuit
- 2.PAGE 11:change the net name of SATA2.3&SATA4.5 to avoid confuse
- 3.PAGE 11: add R564 pull-down resister to LAN_PWROK ,when not use intel lan ,the LAN_PWROK need tied to gnd
- 4.PAGE 12: To change the net of VccCL3_3&VccLAN3_3 power source form VCC3 to VCC3_SB for INTEL LAN W/O F/T
- 5.PAGE 20:Front_USB1&Front_USB2 PIN5 tied to gnd for MCR Device use
- 6.PAGE 22:change VCC5_MS power rail to 5VDUAL to avoid MS have voltage when enter S5 state
- 7.PAGE 24:change VTT_SEL control circuit to follow up 7400 design
- 8.PAGE10& PAGE20:change USB PORT from6&7 port to 10&11 port
- 9.PAGE23:remove EC18 ,add EC76~EC81 for CPU power quility

Ver:0B

2007/11/05

- 1.PAGE 17:Change PWR&SYS resister vaule for FAN linear control circuit
- 2.PAGE 18:Change +12V EL CAP from 1000uf/6.3v to 470uf/16v
- 3.PAGE 21:Change D-SUB RGB Filter vaule for EMI
- 4.PAGE 24:Change PWR&SUS LED power resource from VCC5_SB to 5VDUAL1
- 5.PAGE 11:Reserve D22 for BEEP Noise
- 6.PAGE 11:Modify R387&C503 value of Exrernal RTC Circuit

2007/12/07

- 1.PAGE 1&2&31&32&33:revised north Bridge name form Bearlake- Q to &Bearlake- G (G33)
- 2.PAGE 3:stuff R119 for Wolfdale CPU support
- 3.PAGE 11:unstuff R369 for only one system host allowed on a PECI physical link

Ver:0C

2007/12/31

- 1.PAGE 11:Modify SMSC VBAT power source form VBAT to VBAT_DZ
- 2.PAGE 14:Add C105&C110 (10uf cap) to reduce VTT power ripple current
- 3.PAGE 16:Modify SMSC PECI_READY from FSB_VTT to H_CPURST# for SMSC request to voidl PCEI value incorrect
- 4.PAGE 20:Changed front USB command-mode filter (L44-L47) from 90 ohm to 120 ohm for EMI suggestion

Ver:10


2008/01/30

- 1.PAGE 11:Change lan_disabled source from GPIO34 to GPIO57 for Broadcom WOL issue

Ver:1.2

2008/09/09

- 1.PAGE 16: Add C737 of capacitor to improve the VRM noise for ROPROS-MA and U.
- 2.PAGE 22: Reserve C738 of location to prevent the VRM noise.
- 3.PAGE 22: Reserve C739 and C740 of location to prevent the VRM noise.

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